

Analog Dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

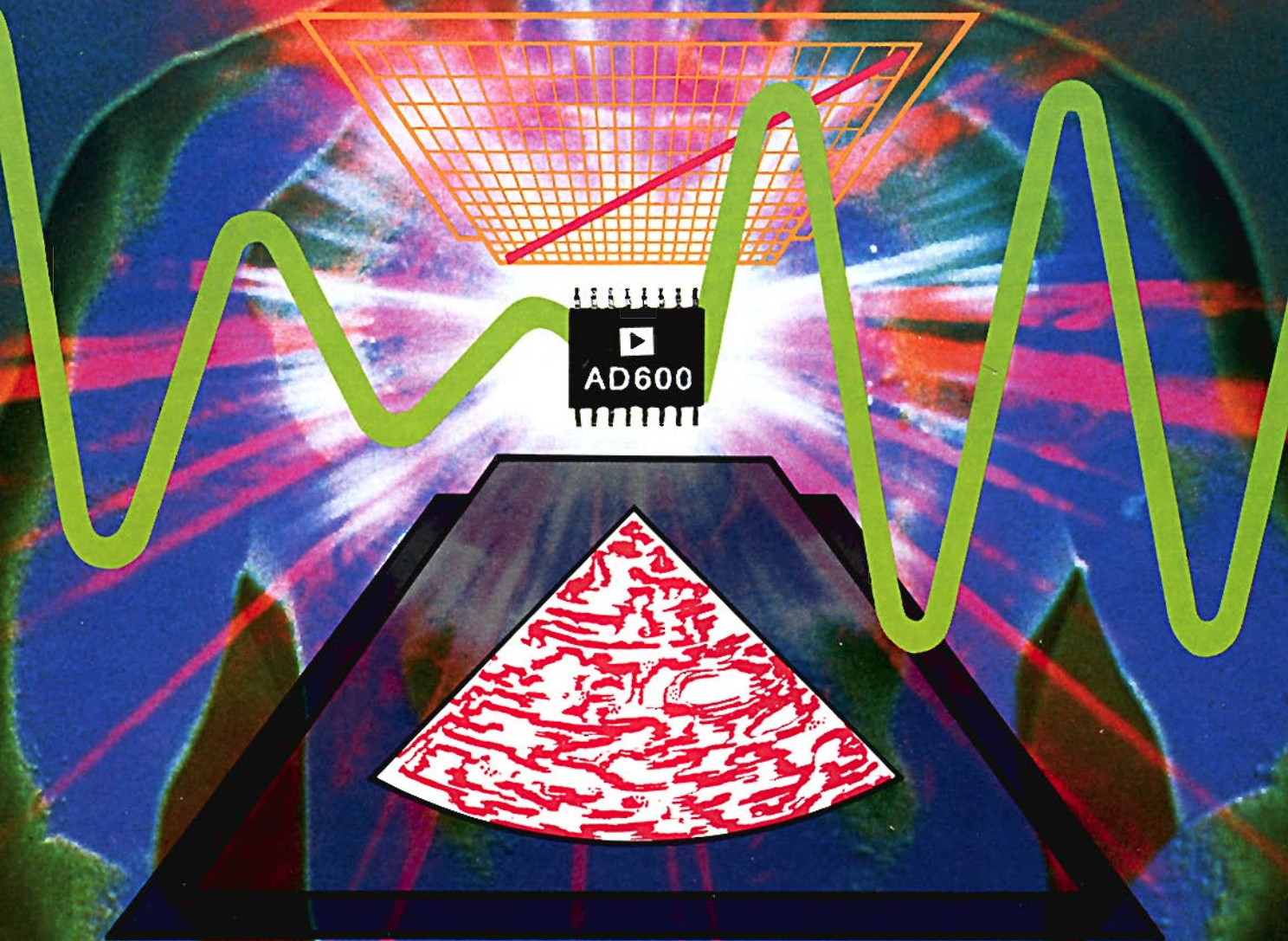
WIDEBAND VOLTAGE-CONTROLLED-AMPLIFIER'S GAIN IS "LINEAR-IN-dB" (page 3)

Signal Computing—Combining hardware chipsets and DSP algorithms (page 8)

3-volt precision op amps available today from Analog Devices (page 7)

Using op amps as line drivers and line receivers (page 13)


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Editor's Notes

SIGNAL COMPUTING


For marketable high-performance systems to process real-world signals digitally in real time for useful purposes, it's getting less cost-effective than ever for a lone engineer—or even organization—to both develop and combine the hardware and software. It seems to make little sense for the engineer who designs a vehicle to reinvent the wheel. The same is true for the system designer in signal processing, whether the “wheel” is a logic gate, an op amp, a high-speed processor and its interface circuitry, a computer “clone”, or a set of DSP algorithms in software.

The article that begins on page 8 describes a cost-effective approach, using “bought” mixed-signal chip sets and software algorithm sets, for multimedia system designers to design and tailor high-performance systems that can both be competitive and contain the designer's unique added value. We call the approach, “signal computing.” All participants—chip manufacturer, algorithm developer, and OEM system designer—are contributing what each does best—in a lowest-cost scenario. 



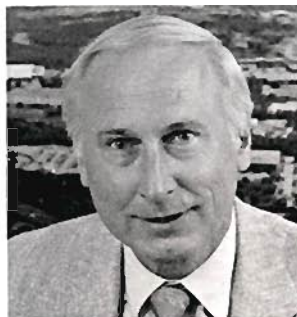
ADBV QUALIFIES UNDER ISO9000

Our Analog Devices BV division, in Limerick, Ireland, has been subjected to a rigorous audit and has received a Certificate of Registration of Quality Systems to I.S./ISO 9001/EN 29001: 1989 from the National Standards Authority of Ireland. ISO9001, promulgated by the International Standards Organization, is the most stringent and comprehensive of the ISO series of standards; for example, the audit surveyed design and customer service, as well as manufacturing.


What does it mean? As the stress on quality grows, preferred vendors to major customers worldwide, including the military, will have to meet—and continue to meet—ISO9000 standards. Analog Devices BV, designers and manufacturers of CMOS integrated circuits, meet these standards now; and other divisions within ADI are in the process of qualifying. 

RAY STATA ELECTED TO NAE

We are pleased to note that Analog Devices cofounder, Chairman and Chief Executive Officer, Ray Stata, has been elected a member of the National Academy of Engineering “for leadership in the development of electronic device technology.”



Election to NAE by its members is among the highest professional distinctions accorded an engineer. Academy membership recognizes distinguished contributions to broad fields of engineering, engineering science and technology, and to the world in which we live.

This honor to Ray as a technological *leader* implies substantial contributions by his *organization*. By reflection, this honors all of the technologists at Analog Devices and acknowledges the significance of the fruits of their labors—documented in these pages for the last 26 years. 

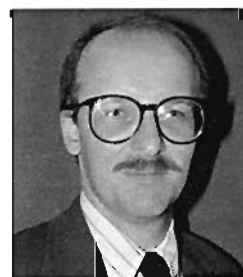
Dan Sheingold

THE AUTHORS

Barrie Gilbert (page 3) an ADI Fellow, is a prolific designer, writer, teacher, and inventor, with numerous patents, publications, and awards. He is also an award-winning Fellow of the IEEE. A native of England, with a degree in Applied Physics (with honours) from Bournemouth Municipal College, he has worked at Mullard and Plessey, and joined ADI from Tektronix. His most visible IC designs have included the AD534 and AD834 multipliers, the AD536 rms IC, the AD537 VFC, & the AD640 log amp.



Bob Clarke (page 3) a Product Marketing Engineer in ADI's Analog Processing Group, with new-product marketing responsibility for analog signal-processing ICs, has a BSEE from MIT. He has worked at *Electronics Test* and *EDN* Magazines, and at M/A-COM. He has written numerous articles for a variety of publications. His hobbies include beer-brewing, windsurfing, and restoring and operating antique amateur radio gear. He is a member of ARRL and IEEE.



Charles Kitchin (page 6) is a technical writer in ADI's Amplifier Group, producing data sheets, technical articles, and sales-support literature. Chuck was graduated with an ASET from Wentworth Institute in Boston and has been studying Electrical Engineering at the University of Lowell's Evening Division. His hobbies include astronomy, wine tasting, and resurrecting lost technologies.



Joe Buxton (page 7), a Senior Application Engineer for the PMI Division of Analog Devices, has worked extensively on the development of SPICE op amp models; he writes application notes and articles for publication and also helps customers resolve their circuit and design problems. In 1988, Joe received a BSEE from the University of California, Berkeley. In his leisure time, he enjoys bicycling, hiking, skiing, and listening to music.



(More authors on page 29)

The cover illustration is by *Shelley Miles*, of *Design Encounters*, Hingham MA.

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106

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Low-Noise, Wideband Voltage-Controlled Amplifiers With "Linear-in-dB" Gain

Low-power, low-distortion, constant-bandwidth AD600 and AD602 duals solve classic VCA problems using new principle

by Barrie Gilbert and Bob Clarke

The AD600 and AD602* are dual-channel low-noise, low-distortion voltage-controlled amplifiers (VCAs). Both devices provide a nominal 40-dB gain range, with a 1-dB overrange at each end; for the AD600, the full range is -1 dB to +41 dB; for the AD602, it is -11 dB to +31 dB. The two amplifiers in each case provide independent gain-control. Their decibel gain is a linear function of the control voltage—"linear in dB"—with an accurate scale of 32 dB/V (31.25 mV/dB).

The amplifier sections can optionally be used for separate signals, cascaded to provide over 80 dB of gain range, or used in parallel to reduce the noise level even further. Their dc-to-35-MHz bandwidth, group delay, and distortion, are essentially independent of the gain. Valuable as time-gain-control elements in sonar and ultrasound, they also provide an excellent general-purpose VCA. They are available in 16-pin plastic DIP and SOIC packages. Their price in either package is \$15 in 100s and \$12 in 1000s.

Variable-gain amplifiers providing linear voltage-control of gain have for years been available in the guise of two-quadrant analog multipliers. They are useful where the gain needs to be varied over a moderate range and noise performance is not critical.

Some applications, however, call for a wide gain range and very low noise. One such example is in medical ultrasonic imaging where an *exponential* gain, controlled by a voltage ramp linear in time, compensates for the exponential decay of the signal with depth of tissue penetration. This calls for gain which is "linear-in-dB." Another example is in automatic gain control (AGC), where the objective is to maintain the output at a predetermined amplitude despite a very wide input-signal range. Because of the closed-loop nature of the control function, the exact gain law is not critical, but the linear-in-dB relationship remains preferable.

THE X-AMP CONCEPT

There are many ways to build a voltage-controlled amplifier—a special case of the more general "variable-gain amplifier," or VGA. The literature goes back to the earliest days of electronics. However, combining wide gain range with constant bandwidth and phase, low noise with large signal-handling capabilities, and low distortion with low power consumption, while providing accurate, stable, linear-in-dB gain has remained an elusive goal.

The AD600 and AD602 achieve these demanding and conflicting objectives with a unique and elegant solution—the X-AMP™ (for

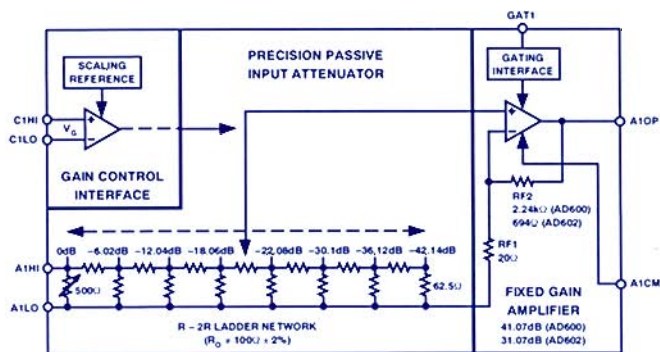


Figure 1. Functional block diagram of one channel of the AD600/602 X-AMP™.

"exponential amplifier"). The concept is simple: a fixed-gain amplifier follows a passive, broadband attenuator equipped with special means to effectively alter its attenuation under the control of a voltage (Figure 1). The amplifier can be optimized for low input noise, and negative feedback is used to accurately define its moderately high gain (about 30- to 40 dB) and minimize distortion. Since this amplifier's gain is *fixed*, so also are its ac and transient response characteristics, including distortion and group delay; since its gain is high, its input is never driven beyond a few millivolts, to further improve these characteristics.

The attenuator is a 7-section (8-tap) R-2R ladder network. The voltage ratio between all adjacent taps is exactly 2, or 6.02 dB. This provides the basis for the precise linear-in-dB gain behavior. The overall attenuation is 42.14 dB. As will be shown, the amplifier's input can be connected to any one of these taps, or even *interpolated* between them, with only a small deviation error—about ±0.2 dB. The overall gain can be varied all the way from the fixed (maximum) gain to a value 42.14-dB less.

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*Use the reply card for technical data. Circle 1

For example, in the AD600, the fixed gain is 41.07 dB (a voltage gain of 113); using this choice, the full gain range is -1.07 dB to $+41.07$ dB, that is, the nominal 0–40 dB is centrally positioned with an overlap of slightly more than 1 dB. The gain is related to the control voltage by the simple relationship

$$G_{dB} = 32 V_G + 20$$

where V_G is in volts. For the AD602, the fixed gain is 31.07 dB (a voltage gain of 35.8) and the central range is -10 to $+30$ dB, with the same 1 dB overlap. Its gain is

$$G_{dB} = 32 V_G + 10$$

The gain at $V_G = 0$ is laser-trimmed to an absolute accuracy of ± 0.2 dB; since this is determined largely by resistor ratios, it is inherently stable with time, temperature-, and supply-voltage variation. The gain *scaling* is determined by an on-chip bandgap voltage reference (shared by both channels), laser-trimmed for high accuracy and low temperature coefficient. Figure 2 shows the gain versus the differential control voltage for both products.

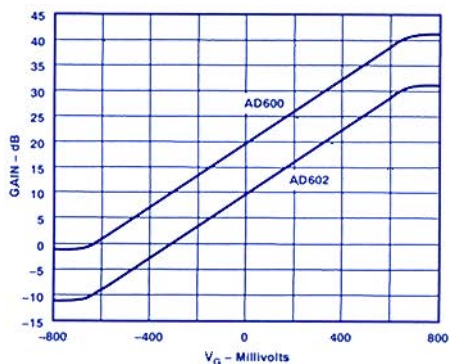


Figure 2. Gain of AD600 and AD602 as functions of control voltage.

To understand how the taps can be selected—and interpolated—under voltage control, let us study the circuit principles further. Figure 3 shows that each of the eight taps is connected to an input of one of eight bipolar differential pairs, used as current-controlled transconductance (g_m) stages; the other input of all these g_m stages is connected to the amplifier's gain-determining feedback network, R_{F1}/R_{F2} . When the emitter bias current, I_E , is directed to one of the 8 transistor pairs (by a means not shown here), it becomes the input stage for the complete amplifier.

When I_E is connected to the pair on the left-hand side, the signal input is connected directly to the amplifier, giving the maximum gain. The distortion is very low, even at high frequencies, due to

the careful open-loop design, aided by the negative feedback. If I_E were now to be abruptly switched to the second pair, the overall gain would drop by exactly 6.02 dB, and the distortion would remain low, because only one g_m stage remains active.

But that's not quite how it's done. Rather, the bias current is *gradually* transferred from the first pair to the second. When I_E is equally divided between two g_m stages, both are active, and the curious situation arises where we have an op-amp with two input stages fighting for control of the loop, one getting the full signal, the other getting a signal exactly half as large! Who wins?

Analysis shows that the effective gain is reduced, not by 3 dB, as one might first expect, but rather by $20 \log 1.5$, or 3.52 dB. This error, when divided equally over the whole range, would amount to a gain ripple of ± 0.25 dB; however, the interpolation circuit actually generates a Gaussian distribution of bias currents, and a significant fraction of I_E always flows in adjacent stages. This smooths the gain function and actually lowers the ripple¹. As I_E moves further to the right, the overall gain progressively drops.

Voltage noise at the input of the X-AMP arises principally in two ways. First, a shot-noise component is caused by the bias current $I_E/2$, flowing in the (noiseless) r_c of each transistor in a pair. This is fundamental and is independent of technology, device geometry, or transistor defects of limitations (such as finite beta). It results in an equivalent noise spectral density (NSD) of

$$e_S = \frac{0.926}{\sqrt{I_E}} \text{ nV}/\sqrt{\text{Hz}}$$

at 27°C, where the tail current, I_E , is expressed in mA. To achieve noise objectives in the AD600 and AD602, a value of 2.4 mA is used, resulting in $e_S = 0.6 \text{ nV}/\sqrt{\text{Hz}}$.

Second, the resistors contribute Johnson noise; its NSD is

$$e_J = 0.129 \sqrt{R_T} \text{ nV}/\sqrt{\text{Hz}}$$

at 27°C, where R_T is the total ohmic resistance associated with the input system—the sum of: the resistance looking into any tap point ($R_o/3$ for an R-2R ladder using a “characteristic resistance” of R_o), the feedback resistor R_{F1} and the sum of the base resistances r_{BB} of any input pair. For the AD600 and AD602, R_T is about 80 Ω , resulting in Johnson noise of $1.15 \text{ nV}/\sqrt{\text{Hz}}$.

¹The interested reader is referred to “A Low Noise Wideband Variable-Gain Amplifier Using an Interpolated Ladder Attenuator,” by Barric Gilbert, IEEE *ISSCC Technical Digest*, 1991, pages 280, 281 and 330. A full discussion of the Gaussian interpolator is found in the same author's “A Monolithic Microsystem for Analog Synthesis of Trigonometric Functions and their Inverses,” IEEE *JSSC* Vol. SC-17 No. 6, Dec. 1982, pages 1179 to 1191.

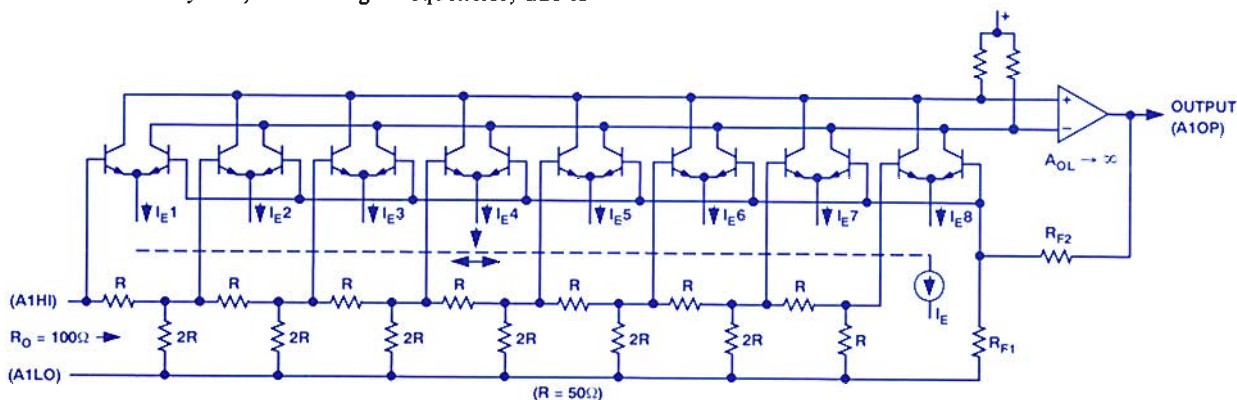


Figure 3. The continuous interpolation between taps is performed with current-controlled g_m stages.

The total input-referred noise is the rms sum of e_5 and e_7 , which amounts to about $1.3 \text{ nV}/\sqrt{\text{Hz}}$. Some small additional noise is attributable to the base currents of the input transistors flowing into the tap resistance and the feedback resistance R_F ; this, and an even smaller second-stage contribution, raise the total input-referred noise to the specified $1.4 \text{ nV}/\sqrt{\text{Hz}}$.

Because the gain of the main amplifier is fixed, the output-referred noise does not depend significantly on the selected gain. Thus, for the AD600, it is $113 \times 1.4 \text{ nV}/\sqrt{\text{Hz}}$, or $158 \text{ nV}/\sqrt{\text{Hz}}$. Referred to its maximum output of 2 V rms, the signal-to-noise ratio would be 82 dB in a 1-MHz bandwidth, or 99 dB in 20 kHz. Since the gain of the AD602 is 10 dB less (but neither the input noise nor the peak output signal differ from the AD600), its noise under all conditions is 10 dB less, that is, an output SNR of 109 dB can be achieved in audio bandwidths.

PRODUCT FEATURES

The AD600 and AD602 include carefully thought-out features to simplify their use in a wide range of demanding applications. For example, the gain-control interfaces are fully differential and at high impedance ($\sim 15 \text{ M}\Omega$ in parallel with 2 pF). A differential interface is versatile: it allows gain to be increased by either a positive or a negative control voltage—and to be readily offset. The light loading facilitates implementation of integrator modes (as in AGC loops—see below) and the simultaneous control of many channels in parallel (as in an ultrasound application). The device needs only 1.25 V for the full 40 dB range, so a simple resistive attenuator and offset can be included to operate this interface, say, from a DAC having a zero to +2.5-V FS output.

The resistance at the signal inputs has to be low to avoid introducing excessive Johnson noise from the attenuator for R_o much greater than 100Ω . On the other hand, the use of these parts is simplified by arranging for this input resistance to be trimmed to a close absolute tolerance ($\pm 2\%$). Thus, when capacitively coupled, the high-pass corner frequency is well-defined. Also, the maximum input voltage can be increased by simply adding a series resistor to form an accurate attenuator, while raising the input resistance. Using a $900\text{-}\Omega$ resistor, a peak input of $\pm 14 \text{ V}$ can be handled; although the noise referred to the new input is ten times greater, the output SNR is unaffected.

The X-AMP™ is based firmly on classical op-amp principles; consequently, the input and output are both referred to the same

ground node. Since it's often valuable to be able to reject a common-mode voltage between the source- and load grounds, input- (A1LO, A2LO) and output-related (A1CM, A2CM) ground pins are included to add this capability for both channels (Figure 4). The amplifiers can drive $\pm 3 \text{ V}$ into $R_L \geq 500 \Omega$, using $\pm 5\text{-V}$ supplies. The distortion specification of -60 dBc holds, even with a $200\text{-}\Omega$ load, for outputs up to $\pm 1.5 \text{ V}$.

Either channel may be independently gated off by a control input; when high, it sets the dc output to within a few millivolts of ground, while greatly reducing the output noise. This is useful in many kinds of beam-forming applications, where channels with a weighting below some level can be switched fully off.

CASCADED OPERATION

The two amplifier sections can be cascaded for a total gain range of 82 dB ($2 \times 41 \text{ dB}$). AC-coupling (Figure 5) blocks the first amplifier's output offset. The maximum gain may be limited by including a resistor at the input to the second attenuator. For example, using 100Ω , the loss at this interface would be $-1-6-1 = -8 \text{ dB}$, and a maximum value of $41-6+41 = 76 \text{ dB}$ for the AD600 (-28 dB to 56 dB for the AD602). The overall bandwidth is about 30 MHz. An optional low-pass filter, C_1R_1 , reduces the noise bandwidth.

With the gain-control inputs connected in simple parallel, the gain scaling is 64 dB/V . However, this does not result in an optimal SNR. To achieve this, the gains may be varied sequentially, by offsetting the gain-control voltages. The first-stage gain increases first, followed by the second amplifier's gain. In this mode, the gain scaling remains 32 dB/V , so a 2.56-V DAC output provides 82 dB of control range. The two sections can also be operated with a 3-dB offset to eliminate the residual gain ripple.

The complete AGC system in Figure 5—with only three active elements—draws on these ideas. Q1 acts as a half-wave rectifier; the average value of its collector current is forced to be equal to the $300 \mu\text{A}$ supplied by the AD590. With R2, it forms an integral bandgap reference which stabilizes the output amplitude to $\pm 1.25 \text{ V}$ with a low temperature drift. This output varies by less than 0.1 dB for an 80-dB input range at frequencies up to 1 MHz, and to within 0.4 dB at 10 MHz. Note that the voltage labeled V_G is actually the *logarithm* of the input amplitude. ▣

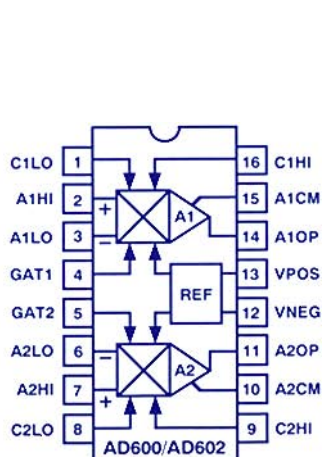


Figure 4. Connection diagram of the AD600/602, showing the shared voltage reference.

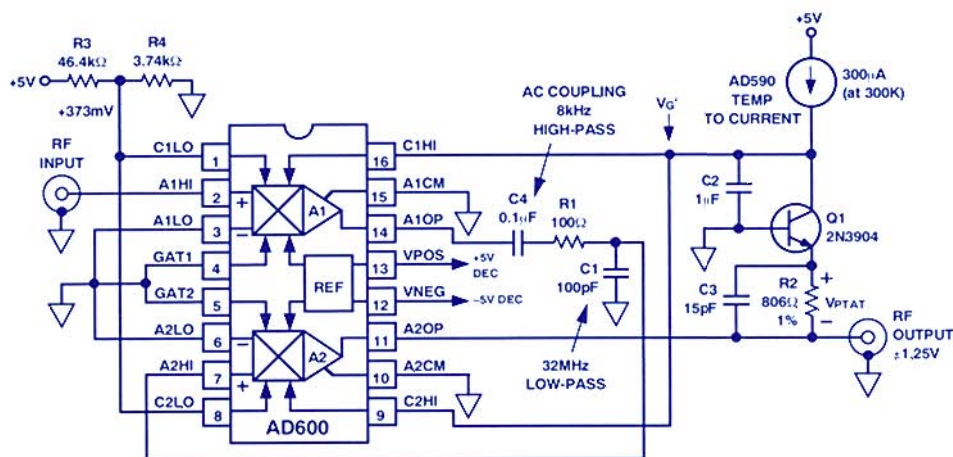


Figure 5. 3-MHz low-noise AGC system with 80 dB or range.

Single- or Dual-Supply Difference Amplifier's Common-Mode Range Exceeds Supply

Monolithic AD626 has pin-programmable gains of 10 & 100, is available at low cost in mini-DIP and SOIC

by Charles Kitchin

The AD626* is a recently introduced monolithic difference amplifier (*Analog Dialogue 26-1, p. 16*), with laser-trimmed fixed gains of 10 and 100 V/V, packaged in an 8-pin mini-DIP or SOIC. Easy to apply, it lends itself well to a wide range of applications. Its low cost makes it attractive for designers to choose this prepackaged monolithic solution in preference to "home-brewed kludges" with multiple op amps. Prices start at \$2.85 (1000s).

The AD626 can be used with either single- (+2.4 to +10-V) or dual (± 1.2 to ± 6 -V) supplies, drawing only 290 μ A, maximum. A robust device, its inputs—buffered by 200-k Ω resistors—are designed to reject a wide range of common-mode voltage, $6 \times (V_S - 1)$ V; for example, with a +5-volt supply the common-mode range extends to +24 V—and to 54 V for a +10-volt supply. With a matched pair of external 2-M Ω resistors in series with the inputs, the CMV range is increased to more than 200 V, with available gains of about 0.9 and 9 V/V. Its output swing (+5-V supply) is from +4.7 V (min) to -30 mV.

Input offset and drift are low, 2.9 mV max over temperature (-40 to +85°C) with 6 μ V/°C max on a single +5-V supply, dropping to 500 μ V max and 0.5 μ V/°C on ± 5 -V supplies (B grade). Common-mode rejection is typically 90 dB (100 Hz, 24 V_{CM}), 80 dB min (B grade). Bandwidth is 100 kHz, and settling time is typically 24 μ s to 0.01% (1-V step, single +5-V supply, or 2-V step, ± 5 -V supply).

With no external elements (except the usual bypass capacitors), the gain is 10 V/V. For gain of 100, a "G = 100" terminal is grounded; for intermediate gain settings, external resistance can be connected in series with it. A "filter" terminal permits a grounded external capacitor to provide first-order filtering.

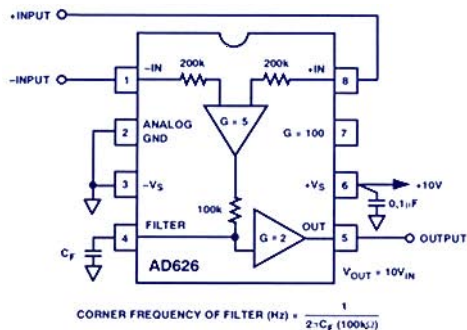


Figure 2. An amplifying one-pole low-pass filter circuit that requires only one external component and operates from a single +10-V supply.

*Use the reply card for technical data. Circle 41

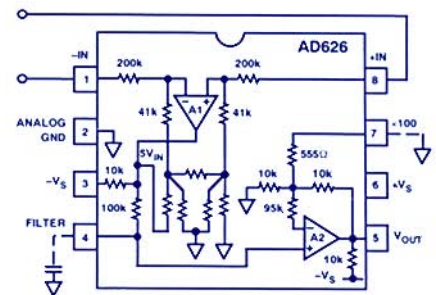


Figure 1. Simplified Schematic of the AD626.

INSIDE THE AD626

The AD626 (Figure 1) consists of two stages—a differential input stage with gain of 5 V/V and an output buffer stage with pin-programmable gains of 2 or 20 V/V—for laser-trimmed overall gain of 10 or 100 V/V. The balanced differential input stage, fed back for overall gain of 5 V/V, includes a resistive input attenuator, which attenuates common-mode voltage to $\times 1/6$ and provides protection against both common-mode and normal-mode overvoltage. The output buffer is connected as a follower-with-gain of 2, provided by a feedback pair of 10-k Ω resistors. An internal 555- Ω resistor, ratio-matched for <1% gain error (0.6% max, B grade), when connected externally to common, brings the gain of that stage up to 20 V/V, and the overall gain to 100 V/V. Intermediate gain values can be provided by external resistance in series (adjusted to take into account the device's $\pm 20\%$ absolute tolerance on resistors); if G is the desired overall device gain the nominal external series resistance value is

$$\frac{50,000}{G - 10} \approx 555 \text{ ohms}$$

Single-pole low-pass filtering can be provided by connecting capacitance to ground from A2's positive input terminal, which is fed from A1's output in series with a 100-k Ω resistance (Figure 2). The nominal capacitance value (C , μ F) for a -3-dB cutoff frequency, f_C , is $1/(2\pi \cdot 0.1 f_C)$.

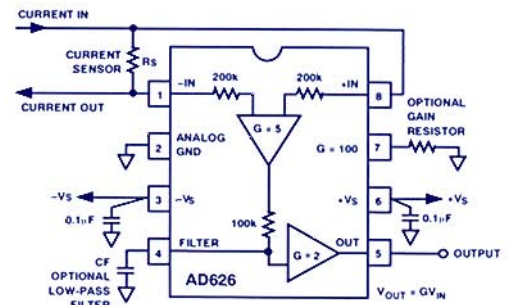


Figure 3. The AD626 operating as a current-sensor interface.

APPLICATION—CURRENT SENSOR INTERFACE

The +54 volt (single supply) common-mode range of the AD626 allows it to be used in a wide variety of applications where a conventional in-amp would not survive. An example is the high-side current sensing interface circuit of Figure 3. The current being measured is sensed by the low-value shunt resistor, R_S , chosen to provide an average differential voltage of about 100 mV.

The AD626 was designed at Analog Devices, Wilmington MA, by Mashe Gerstenhaber, based on an earlier design by Barrie Gilbert. Product test engineering was by Emadeddin Muntasser, trim by Bill Peredina.

3-Volt Precision Op Amps from Analog Devices

An important new trend is developing, and we're already on it

by Joe Buxton

Any reader of the trade journals is aware of recent interest in 3-volt operation of integrated circuits; lowering the supply voltage helps conserve power and increase battery life. Most of the articles have concerned 3-volt-capable *digital* parts for computers. But what about the analog world? Though still in the early stages, interest is growing in op amps that will work with a single 3-V supply for such applications as portable measurement equipment.

Many of ADI's low-power amplifiers can operate at 3 V.* The OP-90 and its dual- and quad versions (OP-290 and OP-490), true single-supply amplifiers, will operate at ≥ 1.6 V. The OP-295, a dual amplifier with guaranteed specifications for operation at 3 volts, will swing rail-to-rail at the output. Still other 3-volt amplifiers, such as the OP-22 and OP-32, can operate on $< 1 \mu\text{A}$ of supply current. Table I shows characteristics of the operational amplifiers, measured with +3-volt (single) supplies.

The actual supply voltage depends entirely on the batteries used in the system. 3 V is commonly achieved by connecting two alkaline batteries in series, but another popular choice is a single lithium battery with a potential of 2.7 V. A third choice may be two or three nickel-cadmium (Ni-Cd) batteries in series, for 2.4 or 3.6-V operation. Ni-Cd and Li batteries maintain a constant potential as they discharge, but alkalines show a significant drop, which needs to be considered. Thus, picking the actual minimum supply voltage for system operation is a decision the designer needs to make based on the characteristics of the batteries used, taking into consideration their cost, capacity, size and weight, shelf life, and discharge characteristics.

At these supply levels, there will be performance tradeoffs. Both input voltage range and output swing are going to be much smaller than for ± 15 -V operation. An important feature of single-supply amplifiers is that their input and output stages can operate linearly down to zero volts. For example, in a dc measurement application, ground is usually used as the reference point and the sensor outputs a signal just a few millivolts above ground. The amplifier needs to amplify that signal accurately with its input-common voltage sitting very close to ground. Both the OP-90 and

OP-295 are capable of this operation. For widest dynamic range, the output needs to swing from ground to as close to V^+ as possible. The OP-295† is excellent in this regard. Its BiCMOS technology provides a CMOS output stage that swings from the negative to the positive rail, along with a bipolar input stage for precision and lower noise.

Not only does limited swing range reduce the largest possible signal, but the noise floor tends to rise, limiting the signal at the low end and further reducing a circuit's dynamic range. Amplifier voltage noise is inversely proportional to the input stage's quiescent current; as current is reduced for less dissipation, noise increases. Adding to this is the resistor Johnson noise in the circuit, directly proportional to the square root of the resistance. In low-power circuits, the resistances—typically large to limit current demands—often generate more noise than the amplifier and need to be considered when evaluating the overall performance.

Low-voltage systems usually require low-power components to extend battery life; this often means decreased speed. Both the small- and large-signal response of low-power amplifiers are considerably less than for higher-supply-current amplifiers. A quick glance at Table I will confirm (yes, that's volts per *millisecond*) that quiescent current is the limiting factor. A voltage feedback amplifier's slew rate is usually limited by the input stage current charging the internal compensation capacitor. Low current means reduced slew rate. The load-drive capabilities will also be smaller. This is not likely to be a concern, because loads in a low-power system should be light. Why pick a low-power amplifier for a circuit where the amplifier has to drive 1.0 V across a 100- Ω load? Also if the capacitive loading is high, the output load current may limit the slew rate.

DC precision is more difficult to achieve for a 3-V circuit than for the same circuit on a 15-V or higher supply. Because the supply is reduced, full-scale input is also reduced. For example, in a 12-bit system with a 10-V full-scale input, 1 LSB is equivalent to 2.4 mV. With 2 V as the full-scale input with a 3-volt supply, 1 LSB is now 480 μV . Thus, errors must be 1/5 as great. But conservative design ensures that precision does not have to suffer because of the lower supply voltage. Such parameters as offset voltage, bias current, and open-loop gain are still excellent at 3 V, as the parameters for the OP-90 show.


Three-volt ICs are gaining in popularity, and Analog Devices offers excellent products to choose from. Besides op amps, ADI offers the AD626 difference amplifier (facing page) and the AD589,§ a 1.23-V two-terminal precision reference. As the technology develops, look for switches (see page 31), an ADC, and other new products to operate at 3 volts. 

Table I. Typical Performance Measured at $V^+ = +3$ V, $V^- = 0.0$ V, 25°C

	Input Range V	Output Swing V ($R_L = 100\text{k}$)	Offset Voltage μV	Open-Loop Gain V/mV ($R_L = 100\text{k}$)	Supply Current (Total) μA	Minimum Supply Voltage for Linearity	GBWP kHz	Slew Rate V/ms	Input Voltage Noise ⁴ nV/ $\sqrt{\text{Hz}}$	Short Circuit Current mA	
OP-295 ¹	dual	0, 2	0, 2.85	200	2000	100	2.0 V	85	30	50	10
OP-90	single	0, 2.4	0, 2.42	125	200	9	1.6 V	17	8	68	25
OP-290	dual	0, 2.4	0, 2.42	125	200	19	1.6 V	17	8	73	23
OP-490	quad	0, 2.4	0, 2.42	600	200	40	1.6 V	17	8	75	22
OP-22 ²	single	0, 2.1	0.5, 2.4	400	500	10	2.2 V	70	7	90	1.0
OP-32 ³	single	0, 2.1	0.5, 2.4	400	500	20	2.2 V	700	60	90	1.0

(All numbers are typical)

1. Guaranteed specifications for 3.0 V are in data sheet
2. Set current = 1.0 μA . The OP-22 has a programmable supply current that can vary from 0.1 μA to 100 μA .
3. Set current = 2.0 μA . The OP-32's supply current varies from 0.1 μA to 1 mA.
4. Spectral noise density measured @ 100 Hz.

*Data sheets for the amplifiers listed here can be found in the Analog Devices 1992 Amplifier Reference Manual, available free. Circle 2

†For complete data on this new product, use the reply card. Circle 3

§For technical data on the AD589, use the reply card. Circle 4

Signal Computing: Hardware Chipsets & Signal-Processing Algorithms Combined

Reprogrammable DSP-based real-world signal-processing OEM applications spurred by new technology and business model

by Bill Schweber

Signal Computing* is a technology framework and business model which recognizes that DSP-based signal-processing applications can benefit substantially by combining sets of high-performance processor- and interface chips with powerful, sophisticated algorithms from independent third parties. Employing open designs and architectures, signal computing is characterized by well-defined levels of standardization that carefully define the hardware and software roles and the layers that make them up.

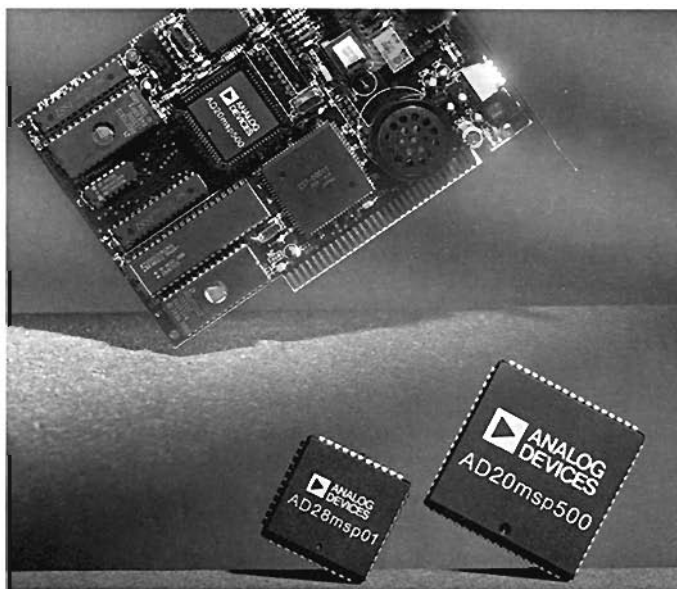
This allows companies—both chip- and software vendors and OEM and system designers—to participate at the level where each brings maximum “value-added” expertise to the application. The chip supplier furnishes standard high-performance, low-cost ICs; the market-oriented algorithm developer provides the standard configurable software that produces the desired electronic performance from the chips; and the OEM designer integrates them into a system specialized to meet the performance needed within his market niche. This environment avoids saddling the designer with the job of recreating all aspects of the overall design. An example of a signal computing product, a telecommunications modem chipset and algorithm toolkit, is discussed later in this article.

Low-cost digital signal processing is an “enabling” function, allowing broad expansion of *real-time* signal processing, through the combination of software and hardware defined as “signal computing.” Signal computing is characterized by the synchronized execution of algorithms on *real-time* data streams. It is quite distinct from the use of DSP, or any processor, in conventional numerical acceleration, where computations and graphics are simply speeded up—but still occur off-line: images are redrawn “more quickly” on the graphics workstation screen, but even though waiting time is reduced, it is still palpable.

In contrast to numerical acceleration, signal computing involves real-time signal processing with a straightforward criterion: if it isn't fast enough for the application's real-time requirements and synchronization, it simply isn't fast enough. Speeded-up processing alone doesn't help if the real-time constraint can't be satisfied.

End users see signal computing functionality (or don't see it because of its transparency) in two distinct forms. First, personal computers (whatever actual form they take) can have signal computing circuitry built in to add those real-time functions (involving intensive computation) that the user needs to access, such as audio, video, and telecommunications capabilities. The software to exercise the hardware for the application must be as available as—or more available than—the hardware, and generally down

*Use the reply card for additional information. Circle 31



loaded into RAM as needed from disk. In this way, new functions can execute on the same hardware, or existing functions can be enhanced with new, more efficient algorithms or incorporate newly defined standards.

Second, in a large number of applications, the signal-computing capabilities are *embedded*, in an essentially non-reprogrammable design, for dedicated use. For example, voice recognition in home “appliances” will be implemented by a carefully defined, fixed-function, minimum-cost subsystem that is optimized for the application, with code in ROM.

APPLICATIONS

As low-cost DSP ICs and interface chips, and the software to drive them, are becoming more widely available, signal computing is spurring a mind-boggling expansion of real-time applications that work with real-world information and signals: voice recognition (including voice-programmed operation of mundane products such as VCRs); spoken-word-to-text and spoken-word-to-spoken-word language translation; personal communications systems; fax-to-OCR-to-voice (so that incoming faxes received at your office can be passed to you over the phone); and voice synthesis that is tailored to the application and the listener. CD quality (44-kbps) will be the standard used for audio and music, except in standard voiceband applications, which don't need the higher sampling rates.

Video has a place among signal computing applications. Under the broad title of “multimedia”—perhaps better characterized as “mixed media”—it allows audio and video to be integrated where appropriate. This means that a video signal, along with its audio channel, can be compressed, stored, transmitted, and re-created with perfect synchronization. Video telephones and conferencing are in the cards—especially for business applications, as a ready substitute for costly and time-consuming travel. Video segments can be stored as easily as typed text is now, and then incorporated into picture-and-sound documents and messages. Video processing allows users to edit images, reducing blurring, improving sharpness, and performing other enhancements with the ease-of-use and power of today's word processors.

THE HARDWARE

The early days of the microprocessor were characterized by a highly fragmented industry without an architectural standard.

Each microprocessor-based design was sufficiently different from others that economies of design standardization could not be realized. The wide acceptance and cloning of the PC-platform changed all that; the core hardware design of each PC is virtually the same. Although each PC design today may use different specific ICs or levels of IC integration, the overall functionality is identical, with the same signal interface functions at the block diagram level.

A similar thing is happening around the signal-computing model. "Reference" designs—complete working schematics and block diagrams—are being made available as chips or sets of chips to provide a standard set of circuit functions. Engineers who use DSP, whether embedded in systems or available with PC-like flexibility, can choose the reference design that has the capabilities they need—and seek out those vendors whose components can implement the design most cost-effectively. Scalable architectures allow more-powerful DSPs (faster clock, more memory) to be used as needed with minimum system-design disruption.

For signal computing, the hardware system consists of three low-cost blocks integrated as a "datapump" (Figure 1):

- the DSP, as the controller and central processor
- the analog front end for interface to the signal source or sink. Examples include the public switched telephone network (PSTN), an audio source and its corresponding output, or a video source and its output
- the signal processing algorithm (usually downloaded and resident in RAM).

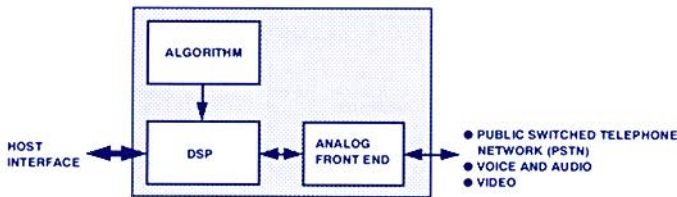


Figure 1. Generalized hardware block diagram.

This datapump supports a host interface for PC-based applications. The DSP and analog front end are available as chipsets, specifically designed to work with each other and compatible with available algorithms. For embedded, dedicated applications the host interface is not needed, and the algorithm is in ROM.

SOFTWARE—OPEN ARCHITECTURE THE KEY

At present, much DSP-related software is custom-fit to the application. This includes the application code itself, as well as the operating system (if any), and the "hooks" to the rest of the system. Libraries and library calls to these libraries are available, but they lack the high degree of standardization found in the PC world with well-defined BIOS and operating system, and related interfaces.

Fortunately, many of the software elements needed to encourage the growth of creative algorithms and software are now taking shape. The final structure is roughly analogous to the 7-layer OSI telecommunications model (Figure 2), which has worked very well at providing flexibility to users by assigning implementation responsibility in well defined blocks, while at the same time assuring transparency between layers. As a result, vendors can offer unique, innovative solutions within each layer—solutions that enhance performance or reduce cost of the total system, yet do not adversely affect the total system structure. While this

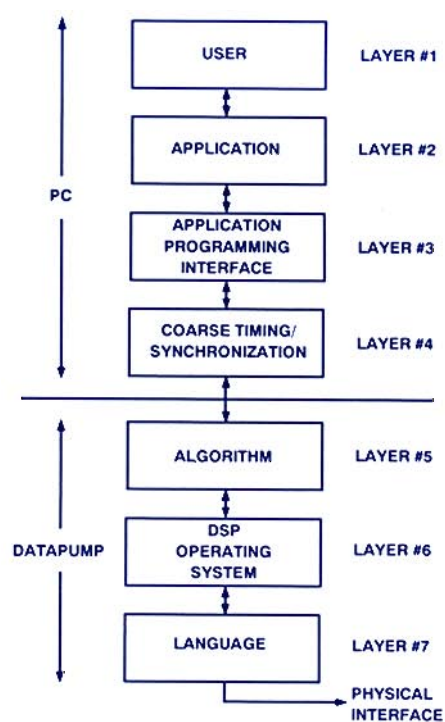


Figure 2. Signal computing layered software structure.

process, when we discuss its details, may sound complicated, it does indeed model a working technology.

The key to this layer structure is its *open architecture*. Each interface between layers is well-defined and distinct. Individual algorithm vendors and complementary software vendors are free to offer their solutions in competition, to meet the challenges of the market and the application. Algorithm vendors provide algorithms to solve specific application needs, such as image compression, audio compression, or telecommunication interface. Software vendors convert these algorithms to code which actually implements these algorithms on specific DSP and chipset platforms.

The "best" hardware and software solution for a particular application is thus determined by the competitive market, since all vendors are free to offer their product on whatever sale or licensing terms they choose. Although DSP IC vendors offer proprietary chip solutions focussed on specific market needs—and will continue to do so—the ferment in the open-system marketplace, involving vendors of ICs, software, and algorithms, will encourage a wider range of innovative solutions.

The upper four layers of the model reside in the PC and its microprocessor. At the top layer is the user interface, for example screen and keyboard. Immediately below is the application, which defines the broad needs of the user. The application program interface (API), layer #3, is where the broadly defined needs are translated into more-specific instructions and service requests. Layer #4 is the PC's operating system, which provides coarse timing, prioritization, synchronization, and scheduling among the various applications requesting service.

The lower three layers, #5 through 7, are implemented by the signal-computing DSP chipset and algorithm. For embedded, dedicated applications, they are the only layers needed. The *algorithm* layer defines how the specific application needs will be implemented in real time. The lowest layer, *language*, provides the set of instructions for the DSP and analog front end as executable code to actually implement the requirements of the

application. The execution of these instructions, with fine resolution timing and detailed resource management, is controlled by the *real-time operating system*.

WHAT IT ALL MEANS

What does all this mean for the industry? It means that new categories of DSP and signal-computing vendors emerge (Figure 3): the independent algorithm vendor, the software vendor, and the DSP O/S supplier. Each provides solutions designed for specific applications, using well-specified open interfaces and architectures at each boundary. The vendors do not have to offer complete solutions at all layers: they need only compete to provide a solution to a part of the problem—for a specific layer.

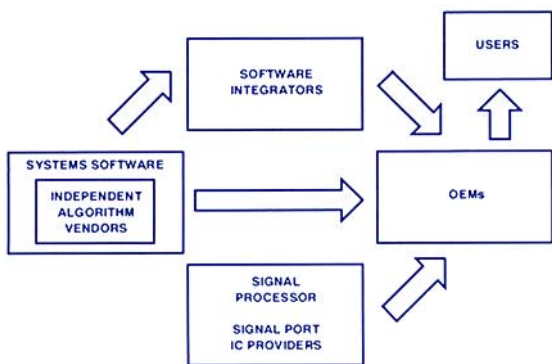


Figure 3. Business model.

Since these independent vendors provide support for all the major DSP families used in signal computing, design engineers are not tied exclusively to one IC vendor. Small, innovative companies also have clear opportunities in the market, since they can leverage their efforts via the path provided by the well-defined layers and open architecture.

What does this mean for the design engineer who must assemble a complete system? In the future, he or she will choose among the various vendors to find a suitable chipset, along with appropriate operating system and algorithms. The project engineer's principal focus will be on system integration. For the many applications with industry-wide standards (for example, JPEG and MPEG image compression and telecommunications), algorithm vendors will offer a variety of solutions. For more-specialized, less-standard niche applications, where there may be only a handful of vendors (of not-totally suitable solutions for the specific problem), the design engineer may find it more cost-effective to develop the algorithm and code as part of the project.

Once the algorithm has been selected, the design engineer can choose between buying the code to implement it, or writing the code as part of the project. Again, the choice depends on the application and the number of vendors. For some applications—such as telecom or voice and image compression—"validated" (tested and verified) code will be available and preferable.

Here's an example: suppose a company that designs answering machines, with expertise in telephone-system line format and protocol, wants to develop a DSP-based, no-moving-part answering machine. The designer can buy suitable algorithms for voice compression, add to these the unique features needed in an answering machine (dial-tone recognition, for example), and so

*Use the reply card for technical information. Circle 42

produce a product leveraging the areas of greatest competence while not "re-inventing the wheel" of voice-compression software.

Signal computing is bringing DSP, a speciality technology, into the mainstream of computing applications. The PC platform brought processor power to both PCs and embedded applications, and created new approaches and business/technology models for system hardware/software design and integration. Similarly, the advent of open architectures and structured layers offers the same opportunity to the processing of real-time signals with DSP as the engine.

SIGNAL-COMPUTING ELEMENTS, EXAMPLE

The AD20msp500 Series of Software Programmable PSTN Communications Chipsets and the ADAT-DS101 Datapump Algorithm Toolkit

These two packages (Figure 4) form a good example of what signal computing technology provides to fill the blocks shown in Figure 1. The chipsets are key building blocks for a variety of low-cost modems and "datapumps." They consist of the AD28msp01 analog signal port for PSTN (public switched telephone network), plus a member of Analog Devices' ADSP-2100 fixed-point DSP family.*

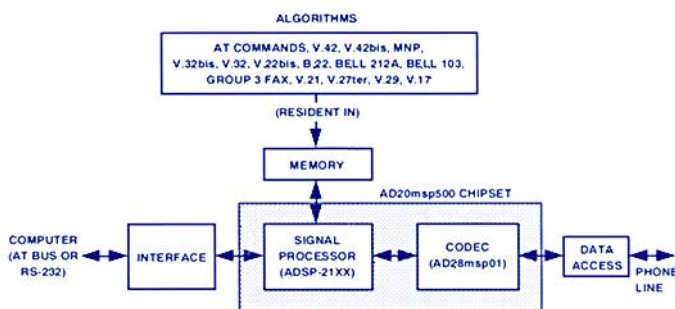


Figure 4. Effective block diagram of telecommunications application (compare with Figure 1).

The signal port is designed specifically for echo-cancelling V.32 and V.32bis modem designs, while the DSP provides processing power to implement algorithms for these standards—plus all fall-back standards, and fax-, data-compression-, and error-correction functions. No microcontroller is used—all functionality is defined and implemented by software; thus the range of functions can be easily upgraded or stripped back (to meet the market needs of the system designer), and any repairs of software defects are easily made.

The toolkit, developed by Digicom Systems, Inc., provides all the software and documentation needed to implement the modem using the chipset. The algorithms can be used "as is" for a standard design—or augmented for applications where customized signal processing algorithms are needed. The toolkit provides the datapump algorithms (which represent telecom standards) as modules; and only the desired modules need be included in the final product.

Available from Analog Devices, the chipsets cost about \$25 in OEM quantities; the toolkit (including a licensing agreement) is \$1,500.

John Croteau and Kevin Leary, of our Norwood, MA DSP group, provided invaluable assistance in the preparation of this article. ■

Dual Op-Amp Has Low Noise and Dissipation, Combines Benefits of JFET & Bipolar Design

OP-275 offers excellent audio specifications, features novel (patented) input circuitry

by Ian Bruce

The OP-275* dual operational amplifier features a novel input-circuit design that merges the best performance features of traditional JFET and bipolar architectures. The result is an op amp that combines their inherent performance advantages—the low distortion and voltage noise of bipolar amplifiers and the high slew rate and wide dynamic range of FETs—for excellence in audio, instrumentation, and consumer applications.

The OP-275 is the first amplifier to feature the “Butler circuit”[†]. The circuit combines bipolar and JFET transistors to provide the accuracy and low noise of bipolar transistors, and the speed and sound quality of JFETs. Bipolar attributes include a low 1/f corner frequency (typical noise spectral density is only 6 nV/√Hz, measured at either 30 Hz or 1 kHz). Total harmonic distortion plus noise (THD+N) is typically 0.0006% (≤ -100 dB), and gain-bandwidth is typically 9 MHz. JFET attributes include a slew rate of 22 V/μs, and combined supply current (both channels) is only 5 mA—one third that of similarly specified devices

BIPOLAR, JFET AND “BUTLER” ARCHITECTURES

IC op amps typically use some form of either bipolar or junction field-effect-transistor (JFET) input circuits. Each has its inherent advantages and disadvantages; and op-amp circuit designers usually base the choice of input devices on the set of performance characteristics needing to be optimized. For example, if slew rate were a prime concern, then JFET inputs would be used, because JFETs generally offer higher slew rates for a given bandwidth than bipolar inputs. On the other hand, if voltage noise needed to be minimized, bipolar front-ends were designed. But what if both slew rate and voltage noise need to be optimized? Typically this can only be accomplished by compromising other specifications, such as power consumption.

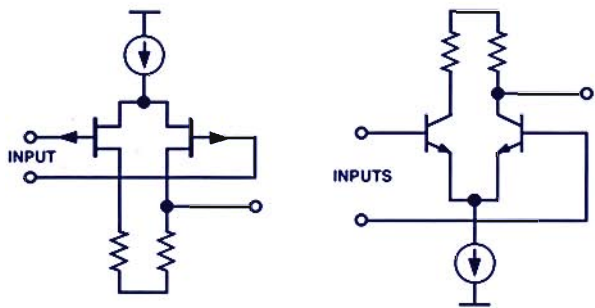
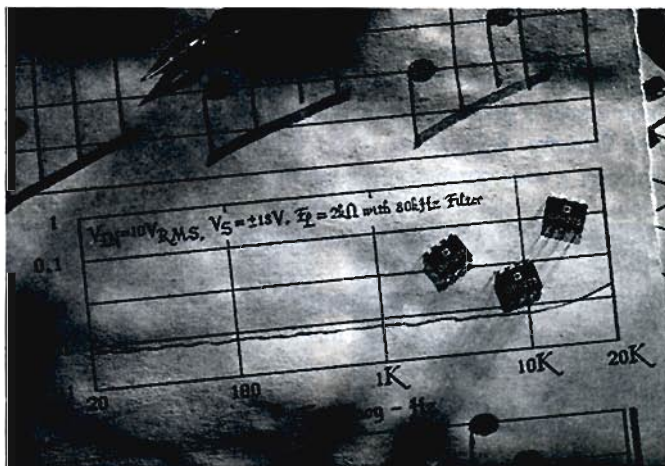


Figure 1. Simplified JFET (left) and bipolar input stages.

*Use the reply card for technical data. Circle 5

†U. S. Patents 5,091,701 and 5,101,126.



The OP-275's new, mixed bipolar/JFET amplifier topology combines many of the performance advantages of both architectures while minimizing disadvantages. To understand the Butler design, let's look at JFET and bipolar designs (Figure 1).

A simplified diagram of a JFET input stage is shown at the left. JFET transistors typically exhibit very high input impedance and lower input bias currents than their bipolar equivalents. Input current noise is lower and slew rates are higher for FETs. More subjectively, JFETs are also thought to “sound good” by many audio professionals. However, along with their relatively low gain, they have somewhat higher input voltage noise and total-harmonic-distortion-plus-noise (THD+N), than bipolar designs.

A simplified diagram of a bipolar input stage is shown at right. Bipolar inputs have much less voltage noise and lower THD+N than JFET circuits. But they consume more power and generally slew more slowly than JFET equivalents.

Figure 2 shows a simplified Butler amplifier circuit. The circuit shares characteristics of both designs. Note that the first-stage bipolar collector currents and the drain currents of the JFETs have been combined. The bipolar circuit's characteristics tend to predominate for smaller input signals, while the JFET circuit predominates for larger signal inputs. This is just as we would want it to be; for smaller input signals, signal-to-noise issues are important and bipolar circuits offer the best specifications; for greater input signals, slew rate is critical and this is where JFETs excel—and where they predominate in this architecture.

The benefits of the Butler topology are best seen by considering transconductance (g_m), a measure of the change in current for a corresponding change in amplifier input voltage. Bipolar circuits typically have high transconductance for small signal swings, but

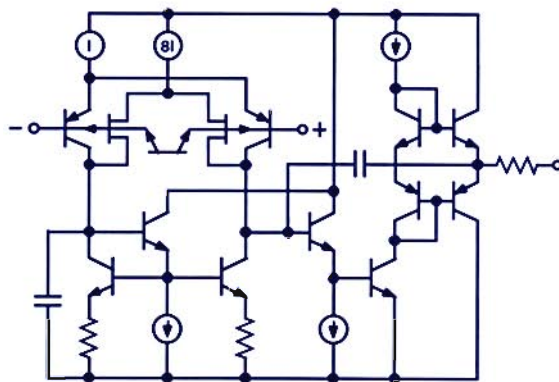


Figure 2. Simplified Butler amplifier circuit.

it drops significantly as the extremes are approached and one of the input transistors tends to "hog" the current. Thus, most bipolar circuits have low distortion for small signals, but when a large signal is presented at the input they enter slew limiting and lose linearity. By contrast, JFET transconductance is relatively flat over a wide range of input signals, so that for higher voltage inputs JFETs can still respond linearly. In the Butler circuit, the FETs take over when the bipolar transistors "run out of gas."

PERFORMANCE CHARACTERISTICS

As mentioned earlier, the very low $1/f$ corner ensures that voltage noise spectral density remains flat at $6 \text{ nV}/\sqrt{\text{Hz}}$ from 30 Hz to 1 kHz. Total harmonic distortion plus noise is well below 0.001% with any load down to 600Ω , although, as with any amplifier, this depends on peak output swing. For low harmonic distortion with large output swings—say 10 V rms output—it is best to increase the power supply voltage. Operating from $\pm 20 \text{ V}$ with a $600\text{-}\Omega$ load, THD+N is below 0.001%.

The bipolar aspect of the input provides quite good dc performance, with offset voltage guaranteed at 1 mV max and typically $< 200 \mu\text{V}$; and bias and offset current compare well with purely bipolar designs. Thus the OP-275 can be used in dc-coupled or summing applications without the expense, crowding, and noise of supplemental offset-adjustment circuitry.

AUDIO APPLICATIONS

It is indeed fortunate that the specifications that interest audio engineers—low noise and THD+N, coupled with high slew rate and low power consumption—are also the virtues of the OP-275. These specifications become especially important in applications such as professional audio equipment and mixing consoles, where numerous op-amps are used in each channel of a multi-channel system.

Op amp distortion and noise errors, though small, are cumulative in each channel; and small improvements in power consumption of individual op amps add up at the system level. For the OP-275, with its maximum supply current of only 5 mA (a third that of comparable devices), in a medium-sized mixing console, this can potentially save hundreds of watts, reducing the size and cost

of the system power supply, and generally improving system reliability.

The OP-275 can also drive capacitive loads of up to 1,000 pF with excellent square-wave response and stability. As a dual, it can be used in stereo buffer/audio line-driver applications such as that shown in Figure 3. With a standard RG-316 coaxial cable having 29 pF/ft of capacitance, the OP-275 will drive more than 50 feet of cable. Figure 4 shows a load-matched scheme for driving a 600-ohm line in push-pull.

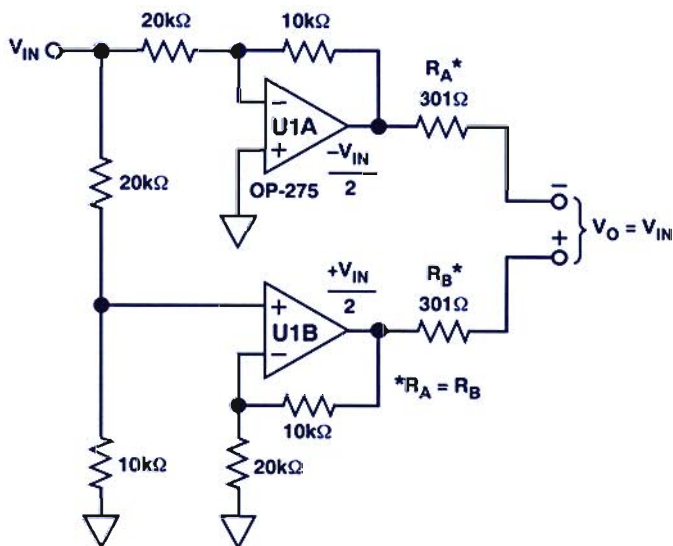


Figure 4. Push-pull audio line-driver circuit for 600-ohm line.

The OP-275 is specified over the extended industrial (-40°C to $+85^\circ\text{C}$) temperature range. It is available in 8-pin plastic DIP and (unlike many audio-amplifier types) SO-8 packages. The OP-275 in SO-8 can offer significant savings in space and manufacturing cost; it can be furnished in 2,500-piece reels for automatic insertion in high-volume applications. Prices start at 99¢ (\$0.99) in 100s.

The OP-275 was designed at Analog Devices PMI Division, Santa Clara, California, by James Butler. ▶

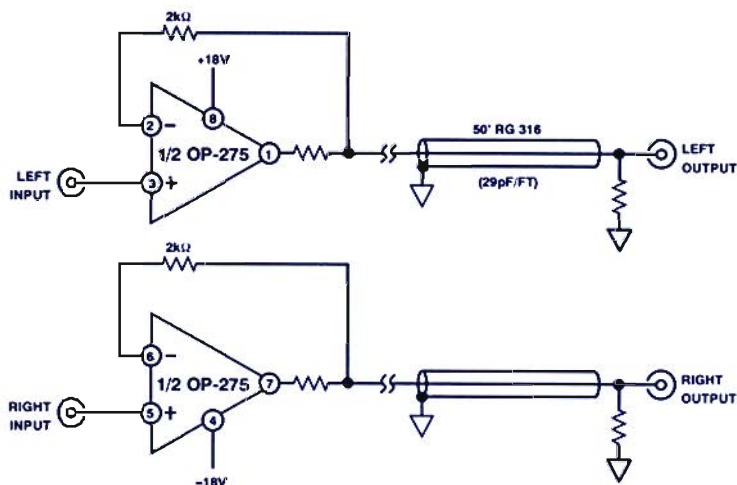


Figure 3. Stereo line-driver configuration.

Op Amps in Line-Driver and Receiver Circuits

Part 1. Video applications

by Walt Jung

INTRODUCTION*

Signal integrity is most-often compromised in the *interconnections* between portions of electronic systems. Audio and video signals have to be transmitted from their place of origin to another location or system with no loss of fidelity. To approach this ideal, careful attention must be paid to layout and grounding techniques, the electrical and physical configuration of the driver and receiver stages, the noise and distortion performance of these stages, and the medium: in the case of wired interconnections, the actual transmission line(s).

Here we look at the design considerations for building line-driving and -receiving circuits—and applying them for high performance in video systems. A future article will discuss how the considerations differ for audio systems.

LINE DRIVERS—GENERAL CONSIDERATIONS

It's usually difficult to design stages to drive lines and remote loads, because they must often handle high current and/or voltage without degrading stability or bandwidth. Current and voltage requirements are fairly straightforward; many IC and discrete devices and circuits are available on the market in with suitable power specifications. But it is no simple matter to use them to drive lines with adequate bandwidth and predictable ac response and dynamic stability—so we will first consider these issues.

It is not easy to achieve adequate performance with capacitive loading—a key design issue because most lines have substantial capacitance. Though achieving stability often involves complex circuitry and reduced performance, standard techniques exist for stabilizing drivers faced with capacitive loads, and they can be implemented in a reasonably direct fashion. The ability to make choices and tradeoffs can help in achieving efficient designs.

Capacitive loading should be looked at in any driver-circuit application, however benign. Signal lead capacitance can build up quickly, even for long runs on a single PC board. Capacitive loading of “off-board” circuits should be evaluated carefully to the degree possible. General-purpose drivers, with outputs intended for the unknown or poorly defined load capacitance of unspecified destinations in the outside world, must be considered a worst case and bulletproofed by appropriate (over-) design.

Overcompensation

A follower-connected op amp with capacitive load is the classic case of a potential stability disaster (Figure 1a). A simple circuit, which could be embodied with most op-amp types, it is a near-worst-case example of a stability-sensitive design. It is likely to respond to pulses with severe overshoots and ringing, if not outright oscillation. What it actually does depends on the op amp's gain- and phase margins with the load in place, a function of the op amp's open-loop response and output impedance (R_o).

*Data sheets for the devices mentioned in this article will be found in the Analog Devices Amplifier Reference Manual, available free. Circle 2

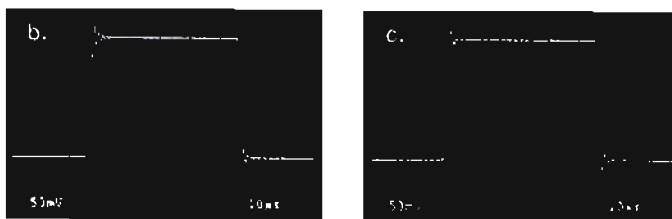
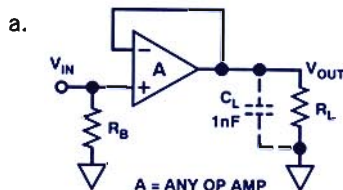


Figure 1. a. Op amp drives capacitive load. Success of application depends on op-amp properties. b. Step response of AD705 with 1-nF load, $C_{comp} = 0$ pF. c. $C_{comp} = 200$ pF.

For example, if the op amp has an open-loop phase shift of 135° near its unity-gain frequency, and if R_o and C_L produce a 45° phase shift in that same vicinity, severe peaking or even oscillation will result. The follower connection tends to maximize this tendency, because it involves 100% feedback. This point is illustrated by the pulse response (Figure 1b) of an amplifier typical of the OP-97 and AD705 families, driven in this circuit with a 200-mV p-p input signal. In this case, there is considerable overshoot and ringing, but no sustained oscillation.

These amplifiers have a terminal (pin 5) that can be used optionally for overcompensation. When additional capacitance is connected from this node to ground, the amplifier's crossover (unity-gain) frequency is reduced, and so is the phase shift at that frequency, restoring a workable phase margin. Here, 200 pF of capacitance damps the ringing substantially (Figure 1c).

Op amps that permit custom compensation can be used in this way to improve stability, but—in addition to the inherent bandwidth reduction associated with most approaches to reducing capacitive load effects—there is a further downside. The amplifier used must allow access to the internal compensation node, an uncommon feature today among precision op amps, such as the OP-07 or AD707. While this is a useful option when available, one must stay flexible and be aware of all options.

Higher closed-loop gain (reduced feedback) will also help stability, following general feedback theory, because phase lag is generally lower at the lower unity-loop-gain frequencies. Therefore, inverters or higher-gain followers (with attenuated inputs, if necessary) will have less tendency to oscillate or peak.

Sensitivity to capacitive loading is not unique to general-purpose feedback amplifiers (Figure 1). “Open-loop” IC buffers and discrete followers can oscillate, given the right combination of source impedance and loading.¹ Like op-amp feedback circuits, they must be isolated from capacitive loads and stabilized.

Compensating for Capacitive Loads Passively

The simplest fix for capacitive loading (Figure 2) is with passive, or “open-loop” circuitry: to isolate the amplifier-circuit's output from the capacitive load, using a series resistor (outside the feedback loop). The load on the amplifier looks like a resistance, R_X , at frequencies above $1/(2\pi R_X C_L)$; although it slightly reduces the amplifier's open-loop gain, it does not introduce additional loop phase lag, and the circuit's stability is less sensitive to C_L . However, the resistance, R_X , causes a voltage drop proportional to

load current; it must be small compared to R_L to minimize low-frequency error. R_X is typically 10-100 Ω , which, for loads ≥ 1 k Ω , produces small (< 1-dB) errors.

The buffer amplifier specs must be consistent with the load requirements—generally for a “muscular” output stage. Table 1* lists salient features of voltage-input [as distinguished from transimpedance] op amps suitable for line driving by virtue of their high speed and current output, and low output resistance. The AD845 in the example of Figure 2 has a minimum gain of 100 V/mV driving loads of 500 Ω and more, and a FET input stage with less than 1-nA bias current. It can deliver up to ± 50 mA of output with an open-loop output impedance of 5 Ω .

Table 1. Voltage Input Op Amps Suitable for Line Driving

Device	R_O (Ω)	BW (MHz)	SR (V/ μ s)	I_O (mA)	V_S (V) ²
AD818	10	150 ¹²	500	± 90	± 2.5 to ± 18
AD840	15	400 ¹²	400	± 50 (min)	± 5 to ± 18
AD841	5	40	300	± 50 (min)	± 5 to ± 18
AD842	5	80 ¹²	375	± 100 (min)	± 5 to ± 18
AD843 ^F	12	34	250	± 50 (min)	± 5 to ± 18
AD845 ^F	5	16	100	± 50	± 5 to ± 18
OP-42 ^F	45	10	50	± 30	± 8 to ± 18
OP-64	30	80 ¹²	130	± 80	± 5 to ± 18
OP-275 ¹	40	9	22	± 30	± 5 to ± 22

NOTES TO TABLE

¹Dual device.

²Gain-bandwidth product, listed at minimum stable gain of:

AD818 & AD842 = 2, OP-64 = 5, AD840 = 10.

³Maximum ranges shown.

^FFET input device.

For low-impedance loads, such as 500 Ω for R_L , a series resistance, R_X , of 50 Ω produces a 9% gain error, which often requires correction for unity overall gain, either locally or elsewhere in the system. It can be achieved locally by using feedback resistors in the same ratio, R_X/R_L ; accuracy of the overall gain will depend on whether R_L is constant. If the circuit is already connected for gain, the required correction means revising resistance values for a $(1 + R_X/R_L)$ gain increase.

This series- R_X capacitive-load compensation technique, though generally effective and quite simple, does have drawbacks:

- Loss of gain (or gain accuracy): used with a fixed-gain stage, it causes a gain/power loss, which will vary with loading. If the load is known and stable, the low-frequency gain error—as well as corresponding cable losses—can be optionally compensated.
- Loss of bandwidth: This technique (like almost all others to isolate capacitive loads) also causes a loss of frequency response, a loss likely to be serious with high-speed amplifiers. For this example, the effective bandwidth will be about 3.5 MHz, well

below the basic 16-MHz bandwidth of the AD845 op amp. In essence, the bandwidth will be limited to $1/([2\pi C_L(R_X \parallel R_L)])$.

- Loss of slew rate: The capacitive load can limit the slew rate (SR). In general, the inherent SR of the amplifier will be reduced to $I_{O(max)}/C_L$ volts per second. For example, while the AD845 has a basic SR of 100 V/ μ s, the ± 50 -mA output-current limits cause it to fall to about 50 V/ μ s with $C_L = 1$ nF. The SR is subject to the uncertainty of the amplifier’s short-circuit current limit, which usually varies inversely with temperature. *This general limitation will apply to any capacitively loaded amplifier and is particularly acute in high-slew-rate devices.*

The general technique of Figure 2 can be used with most amplifiers. The higher-speed, ± 100 -mA-output AD842—manufactured on a complementary bipolar (CB) process—provides more current to a load, but it must be connected for a closed-loop gain of at least 2 V/V. This can be done without affecting the low-frequency gain by connecting an appropriate “dummy” noise-gain resistor between the amplifier’s \pm inputs. (R-C networks can also be used, avoiding an increase in output dc offset—but possibly increasing settling time.)

With transimpedance amplifiers, even higher current drive is available—up to ± 150 mA, for the AD811,³ connected as shown in Figure 3.

This circuit, similar to Figure 2, is configured differently for gain, because the AD811 is a transimpedance amplifier. When they are used as non-inverting gain stages, the value of R_F is fixed, and R_{IN} ’s value is set to adjust the gain. For the conditions of Figure 2, R_F is set at 750 Ω ; for a simple voltage follower, R_{IN} is left open. To correct for the output attenuation, R_{IN} is 30.9 k Ω .

Unlike voltage-input op amps, transimpedance amplifiers prefer an optimum value of R_F for flat frequency response—a function of supply voltage, closed-loop gain, and device type. For the AD811 at a gain of +1, it is 750 Ω . With other devices, the R_F value specified on the device’s data sheet should be used.

The AD811 also permits R_F to be increased to improve capacitive load-handling for $R_X = 0$, but with less-flat frequency response. With $R_X = 12$ Ω , as shown, response is optimized into a 1-nF load⁴. The AD811 has major benefits in this application, since the bandwidth is increased (over Figure 2) to 13.5 MHz. The ± 150 -mA short-circuit output drive of the AD811 increases the circuit’s SR to 150 V/ μ s (much less than its unloaded 2500 V/ μ s spec, but much more than that of Figure 2).

Transimpedance amplifiers, used as in Figure 3, tend to have poorer dc and low-frequency performance than conventional op amps. Common-mode errors can be minimized by using the

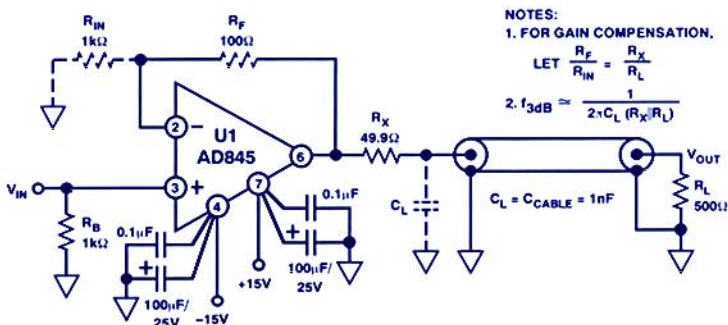


Figure 2. Open-loop series resistance isolates capacitive load in voltage-input op-amp circuit.

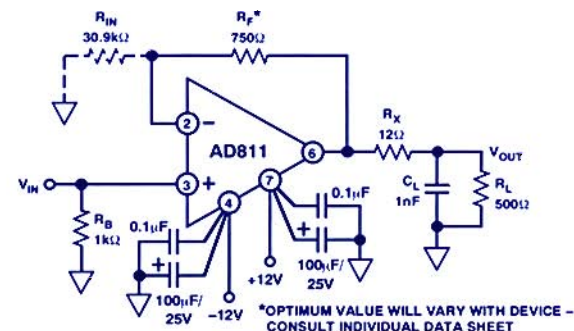


Figure 3. Open-loop series resistance isolates capacitive load in transimpedance op amp circuit.

amplifier as an inverter, rather than as a follower (when possible), or as a high-current buffer with another op amp in a composite stage (Figure 7 below). Finally, the AD846 is a transimpedance op amp with precision dc characteristics.

Table 2* illustrates the specs of a variety of transimpedance op amps that are relevant to use as line drivers. Similar R_F and R_{IN} selection considerations to those discussed above would apply with other transimpedance amplifiers when used in this circuit.

Table 2. Transimpedance Amplifiers Suitable for Line Driving

Device	R_F (Ω) ⁴	BW (MHz)	SR (V/ μ s)	I_O (mA)	V_S (V) ⁵
AD810 ¹	750	100	1000	± 75	± 5 to ± 18
AD811	649	120	2500	± 150	± 5 to ± 18
AD844 ²	499	60	2000	± 80	± 5 to ± 18
AD846 ²	1k	80	450	± 65	± 5 to ± 18
AD9617	402	190	1400	± 60	± 5
AD9618	1k	160	1800	± 60	± 5
OP-160 ¹	825	90	1300	+60/-45	± 5 to ± 18
OP-260 ³	2.5k	90	1000	± 50	± 5 to ± 18

NOTES TO TABLE

¹DISABLE pin available.

²Compensation node available.

³Dual device.

⁴Optimum value will vary with supply voltage.

⁵Maximum values shown.

Internal Capacitive-Load Compensation

A simpler approach is to use an op amp designed to handle capacitive loads without requiring external compensation. Table 3* lists a number of available amplifiers with this internal feature.

Typical of such amplifiers are the AD847 and AD817. In these devices, part of the amplifier compensation network is a capacitor, C_F , connected to feed forward around a unity-gain output stage. In normal circuit operation, this capacitor has little effect; but with capacitive loading and large signals, a current is drawn from the output and a voltage drop appears across the C_F network, accompanied by current flow. This in effect adds additional capacitance to the device's internal compensation, effectively slowing the amplifier's response.

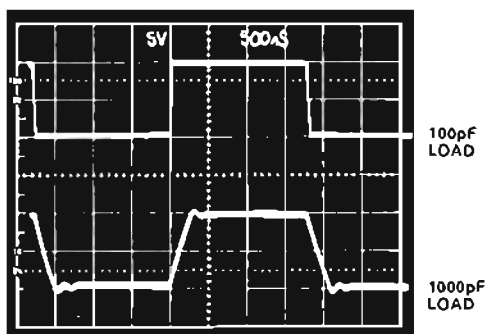


Figure 4. Large-signal response of amplifiers with internal compensation for capacitive load (AD847, AD817).

Figure 4 shows a typical large-signal response for 100-pF and 1000-pF loads. The small capacitive load (top) allows fast output swings, while the larger capacitance (bottom) slows the output rate of change, but without instability. The compensation is *adaptive*, coming into play as needed, as either loading is increased or the output moves more quickly. This results in simpler applications; stability issues due to output capacitive loading arise less frequently, allowing attention to other details.

Some caveats associated with internal compensation:

- Loss of bandwidth: As with passive compensation, bandwidth decreases (depending on the application) as the device slows down to prevent oscillation as load current flows.
- Signal-level dependency: The compensation network has its greatest effect when enough output current flows to produce voltage across C_F . Conversely, at small signal levels the effect of the network on speed is much less, so greater ringing may actually be possible for some circuits for low-level signals.
- Distortion: Because the circuit is based on a nonlinear principle, the internal network affects distortion and the ability to drive loads; this factor impacts amplifier performance in video applications. Though it doesn't make amplifiers such as the AD847 or AD817 unusable for video; it precludes the very lowest levels of distortion achieved by otherwise comparable amplifiers (some examples will illustrate this point).
- No "free lunches!": The approach can help greatly, but it is not a panacea. Though an op amp of this type may solve the loading problem, the design is not freed from instability from *other* sources (such as input capacitance, feedback and PC-board strays). These still need to be considered—as for any application.

In sum, internal capacitive load compensation can be a great utility feature, making applications easier to get up and running. But when the limits of performance are pushed, other amplifiers, and more-comprehensive approaches, may be better choices. Table 3 lists some amplifiers with internal capacitive load compensation.

Table 3. Amplifiers with Internal Capacitive Load Compensation Suitable for Line Driving

Device	BW (MHz)	SR (V/ μ s)	I_O (mA)	V_S (V) ⁵
AD817	50	350	± 90	± 2.5 to ± 18
AD827 ¹	50	300	± 32	± 5 to ± 18
AD829	NA ^{2, 3}	230	± 32	± 5 to ± 18
AD847	50	300	± 32	± 5 to ± 18
AD848	175 ⁽³⁾	300	± 32	± 5 to ± 18
AD844 ⁴	60	2000	± 80	± 5 to ± 18
AD846 ⁴	80	450	± 65	± 5 to ± 18
OP-160	90	1300	+60/-45	± 5 to ± 18

NOTES TO TABLE

¹Dual device.

²Bandwidth varies with compensation.

³Gain bandwidth product, listed at minimum stable gain of: AD848 = 5, for AD829 @ $G = 20$, BW = 50 MHz (can be compensated for $G = 1$).

⁴Cap load compensation optionally available externally (see data sheet).

⁵Maximum ranges shown.

External Capacitive Load Compensation

External, or "in-the-loop" compensation is the most flexible and accurate general way to isolate/compensate capacitive loads. It is flexible; in principle, it applies to any unity-gain stable op amp, in inverting or noninverting operation. It is accurate; the isolation resistor is included within a dc feedback loop for excellent low-frequency gain accuracy, independent of the load and limited principally by the circuit's gain resistors (assuming adequate op-amp gain). Unfortunately, like other techniques discussed thus far, it also reduces bandwidth and slew rate.

Figure 5a illustrates the principle. In this circuit, a noninverting gain-of-2 stage, resistor R_X isolates the capacitive load C_L . Unlike Figure 2, the feedback return is taken from the *load* side of R_X ,

*Data for the devices mentioned in this article will be found in the Analog Devices Amplifier Reference Manual. Circle 2

enclosing it within the loop; this automatically corrects gain errors caused by loading at the lower frequencies. The gain expression is like that of a standard noninverting op amp stage.

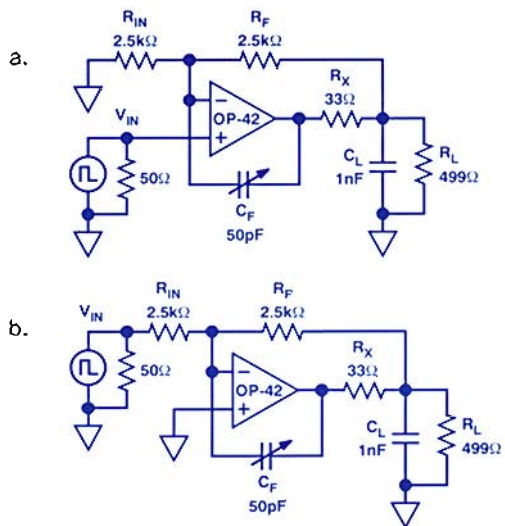


Figure 5. a. Inside-the-loop compensation of non-inverting stage using voltage-input op amp. b. Inverting version of (a). Dynamically, capacitor C_F provides compensation for the additional lag introduced by the R_X - C_L combination. For a given set of values, C_F can be adjusted to cancel much of the destabilizing effect of C_L and provide a well-damped step response, countering the tendency towards overshoot, ringing or oscillation. Bandwidth is reduced; the closed loop bandwidth of this stage is a function of R_F and C_F , as well as R_X and C_L . The value chosen for R_X is not highly critical, but it should be kept small to avoid degrading power output and bandwidth; the stage can be tuned with values in the range of 10-100 ohms.

The optimum value for C_F is a function of R_X , C_L and the gain resistors; with fixed values for R_F , R_{IN} and R_X , it will track C_L . While several references suggest procedures for predicting C_F ,^(2, 6) a practical approach is to select a close nominal value for C_F , then adjust it for optimum pulse response in the final circuit layout.⁷ This approach, taking into account additional parasitic capacitances, was used in the examples discussed.

To minimize sensitivity to stray capacitance, it helps to keep the values of R_F and R_{IN} low. The resulting higher values of C_F , typically >20 pF, will be more predictable and stable. C_F is best made up of an NPO capacitor in parallel with an NPO trimmer. Optionally, once the optimum value is verified in a final layout, a single fixed value can be used. The following examples use ± 15 -V power supplies (bypassed as noted in the sidebar).

Figure 6a shows the well-controlled response of the circuit of Figure 5a—with an OP-42 driving a 1-nF load—to a 200-mV p-p small-signal pulse. As C_F (or C_L) is varied away from this opti-

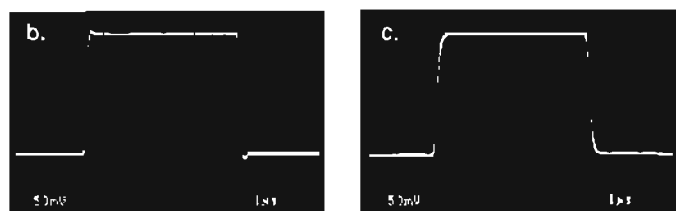


Figure 6. a. Small-signal response of Figure 5a b. Small-signal response of (5b).

um, the displayed response (not shown) tends towards increased overshoot for higher C_F/C_L , and towards overdamped, for lower C_F/C_L . This compensation technique is a good one to tune this circuit for guaranteed stability. If the maximum C_L is known, the stage can be tuned to accommodate it, and lower C_L values make it slower and more stable.

A related unity-gain inverting circuit is shown in Figure 5b. It uses the same values and has the same noise gain as the circuit of Figure 5a. 6b shows the well-controlled pulse response for the same 200-mV p-p output level and 1-nF load capacitance.

When tailored properly, the output and compensation networks can influence bandwidth and SR more than the device used. For example, AD845 and OP-275, tested in these circuits, gave small-signal results quite similar to those shown in 6a and 6b.

When the required current output exceeds a given op amp's specs, an "inside-the-loop" buffer can be added. For example, Figure 7a shows a non-inverting application—like Figure 5a in concept—where an AD811, connected as a unity-gain buffer, is interposed between the U1 and the load to boost the current output up to ± 100 mA (± 150 mA peak). U2 drives the load—instead of the output stage of the U1 amplifier.

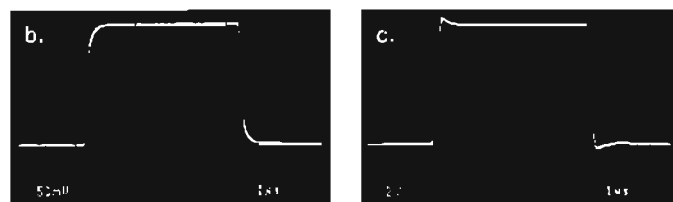
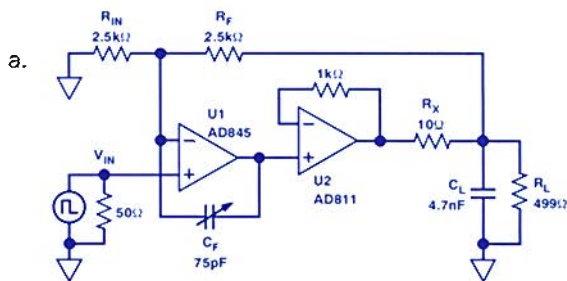


Figure 7. a. Inside-the-loop compensation of buffered non-inverting stage using ± 100 -mA current-feedback op-amp as unity-gain buffer. b. Small-signal response. c. Large-signal response.

While the basic compensation components function as before, R_X is decreased to 10 ohms to allow greater loads to be driven, in this case 4.7 nF|499 ohms. Figures 7b and 7c show the circuit's response to small- and large signals. Because of slew-related lag, the circuit cannot be identically compensated for both large and small signals; with C_F adjusted for slightly overcompensated small-signal response, the large-signal response shows just a small overshoot. The 150-mA current limit of the AD811 can slew the 4.7-nF load at about 30 V/ μ s.

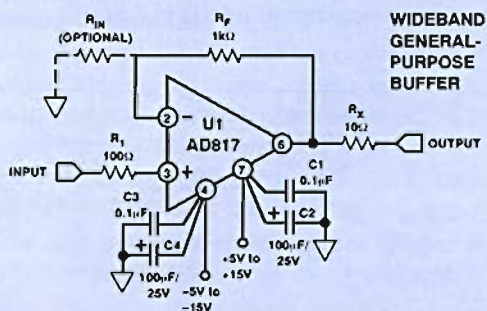
Figure 8a shows a buffered inverting circuit with the same loading; small- and large-signal responses are seen in 8b and 8c. As before, the small-signal response is well controlled; the large-signal response is slightly less damped, due to the slew lag.

These external compensation techniques for op amps are widely applicable; with proper adjustment, they provide compensation without much reduction of bandwidth and SR. This technique can be used with a variety of devices, buffered and unbuffered.

(continued on page 18)

CHOOSING IC AMPLIFIERS FOR HIGH-PERFORMANCE BUFFERING

Buffer stages are widely used in analog circuits and systems to preserve signal accuracy by unloading high-impedance circuits—and to drive difficult loads. Buffer stages are typically configured as voltage followers—non-inverting unity- (or low) voltage-gain stages, with high current gain. For example, this general-purpose buffer circuit works with many IC amplifiers, with or without overall loop feedback—as needed.



Available IC forms of buffers are generally “open-loop”—non-feedback—types. They typically operate with slew rate (SR) of a few hundred V/μs, gain-bandwidth of up to 100 MHz, load-drive down to 100 ohms at current levels of up to 100 mA, with low distortion and stable gain. DC performance (gain accuracy, offset and drift, and input impedance) is often secondary—which can limit their overall utility (or require dc stabilization).

OP-AMP BUFFERS

DC and low frequency specs are the strength of conventional (vs. transimpedance) op amps. They have low offset, bias current, and common-mode errors (including power-supply sensitivity). However, speed is relatively poor because of limited slew rate and bandwidth. The limits become most acute when conventional op amps serve as unity-gain voltage followers.

Nevertheless, selected devices are notable for providing a useful combination of specs (see Tables). Of these, perhaps the best overall utility is provided by the AD817 or AD845. With conventional op amps, the above buffer circuit does not need R_F as a follower, but can use both R_F and R_{IN} , should gain be desired. Interestingly, the AD817, with $R_F = 1\text{ k}\Omega$, as shown, maintains gain flatness up to 70 MHz in this circuit.

In general, besides the ultimate slew rate due to limitations on the charging rate of internal capacitances, the output-current-limited slew rate of this buffer (and those discussed below), operating into a capacitive load with a short-circuit current, I_{max} , will be as discussed with the circuit of Figure 2.

OPEN-LOOP BUFFERS

In contrast to conventional op amps, open-loop buffers and transimpedance, or current-feedback, amplifiers operate without internal slew-rate limitations. Not needing overall lag compensation, open loop buffers tend to be much faster. The traditional tradeoff here has been speed for accuracy, which tends to be worse without corrective loop feedback. The BUF-03, for example, has no loop-feedback corrective gain mechanism (although the novel hybrid output stage does minimize dynamic errors).⁹ More-recent bipolar buffer designs, such as the AD9620 and AD9630, achieve excellent accuracy of up to 0.995 V/V, but with a proprietary closed-loop topology.

The strength of the BUF-03 lies in its very low input current (150 pA), low offset voltage (2 mV), and high output current of

$\pm 70\text{ mA}$. When standing alone, it requires no external circuitry, except for offset nulling—if desired—and the usual bypassing.

TRANSIMPEDANCE AMPLIFIER BUFFERS

Transimpedance (or current-input) amplifiers provide an intermediate answer to the speed/accuracy question. As a rule, they perform much better than voltage-input devices for high-speed applications. The transimpedance amplifier's feedback mechanism has much less of a tendency towards slew limiting and closed-loop bandwidth changes much less with increasing gain. So, transimpedance amplifiers dynamically are more suitable than conventional op amps for follower-type buffers.

Transimpedance amplifiers generally have better gain accuracy than open-loop designs. In contrast to 1% gain errors for some open-loop designs, a good transimpedance buffer can have unity-gain error of the order of 0.1% (a gain of 0.999) with loads well below 1 kΩ. Higher gains are also available by appropriate choice of resistance ratios.

A transimpedance amplifier as a unity-gain follower (R_{IN} open) in the buffer circuit shown above allows maximum flexibility for gain and load drive. This circuit must use a feedback resistor (R_F), specific for a given device (Table 2). To configure the buffer for gains greater than unity, add an appropriate R_{IN} .

The AD811, especially useful for driving heavy loads, due to its high output current, is optimum from a speed/power point of view, with a 2500 V/μs SR, $\pm 100\text{-mA}$ output current, and more than 100 MHz of bandwidth. The gain error of an AD811 voltage follower, with a 1-kΩ R_F will be 0.067%. The dc performance is still attractive; Input offset voltage of the AD811 is typically 0.5 mV; bias current is 2 μA.

DC performance of the above circuit of is also limited by the CMR and PSR of the device: 60-70 dB for the AD811. For critical situations, the AD846 can be used. It has 125 dB of CMR and PSR and an R_T of 200 MΩ. In the same circuit, gain error of the AD846 will be 0.0005%, representing two orders-of-magnitude improvement.

GENERAL NOTES ON BUFFER STAGES

Regardless of which IC is employed, close attention should be given to minimizing parasitics in buffer stages, at input, output, and supply terminals. Buffers should follow the rules for physical construction of high-speed circuits. A solid, heavy copper ground plane should be used, and circuit layout should be compact, with low capacitance around high-impedance nodes. Signal runs and grounds should be laid out with signal coupling and load-current flow in mind.^{10, 11}

If the load will not be source-matched to a cable with a 50-100 ohm termination for R_X , then R_X should be $\geq 10\ \Omega$, to isolate capacitive loading (see text). Some amplifiers may require an input parasitic suppression resistor (R_1) (see device data sheets).

Power supplies should be well bypassed close to the high-current IC pins. Low-inductance/low ESR rf bypass caps (C_1, C_3) should be used right at the pins. These are 0.1-μF surface-mount chips (or other low-inductance types). For driving high peak-current loads, these bypasses should be augmented by short-lead high-capacitance, low-ESR electrolytics ($C_2, \& C_4$, 47-100 μF). As they carry transient currents, they should be rated for high frequency (viz., switching-supply types). →

DC power management and dissipation are also important with buffer ICs, which can dissipate fairly large power levels at light loads. For example, the AD811's quiescent current drain is 15-18 mA. So a heat sink should be used for supplies $> \pm 12$ V. To minimize power and temperature rise, note that video and other low-voltage-swing applications can use ± 10 - 12 -V supplies. For buffer circuits needing a full ± 15 V, use the lowest-possible-thermal-resistance package, and add an appropriate heat sink (Thermalloy 2227 for the BUF-03 or other TO-99 ICs, AAvid #5801 for the AD811 or other 8-pin ICs).

Because of this stage's very wide bandwidth, low phase shift, and low output impedance, a fast buffer can either "stand alone," as shown here, or serve as a more-conventional "inside-the-loop" buffer, to minimize loading on a high-precision amplifier. For any conventionally rated-output amplifier this can be a salient improvement; it can increase the linear output drive to $\geq \pm 100$ mA, while maximizing linearity, preserving gain, and reducing distortion. The Tables show a number of amplifiers suitable for buffers.

(continued from page 16)

The circuit examples can be used as shown here; but please also note that similar capacitive-load compensation architectures, with the values optimized for specific devices, are shown on many of our op-amp data sheets.

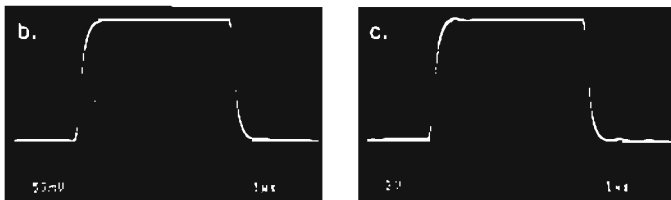
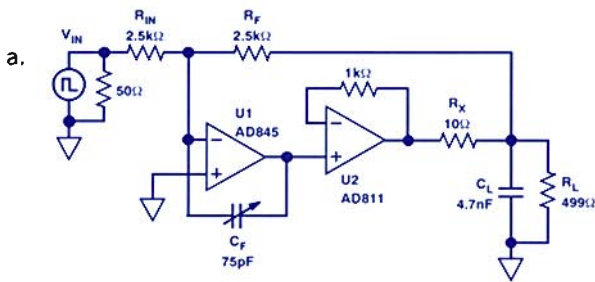


Figure 8. a. Inverting version of Figure 7. b. Small-signal response. c. Large-signal response.

Source/Load-Terminated Transmission-Line System

The capacitive-load compensation techniques described above are hardly a perfect solution to the line-driving problem. Perhaps the best and most foolproof way to drive a long line (which would otherwise present substantial capacitive load) is to treat it as a source- and load-terminated transmission line—a standard for many years in video- and rf-system signal distribution. With proper termination, bandwidth limitations are greatly reduced.

Figure 9 shows a basic wideband video driver, configured to drive a video line and a remote load, R_L , with a 1-V p-p signal. With a matched, wideband transmission line, such as a 75-ohm coaxial cable, the capacitance of the line is not seen directly by the amplifier. Instead, as a distributed-constant transmission line, it has a characteristic impedance, Z_0 ,¹¹⁰⁾ where $Z_0 = \sqrt{L/C}$.

When source and load impedances, R_T and R_L , are equal to the nominal Z_0 , in this case 75-ohms, the loading presented to R_T at the input side of the line is a 75- Ω resistance. The line is nominally flat in frequency response, within the tolerance of its transmission-line design parameters. The amplifier sees an effective resistive load of R_T plus R_L , in this case 150 Ω . The attenuation from amplifier output terminal to the load is 2:1; system bandwidth is determined principally by the amplifier. To deliver 1 V p-p to the load, the amplifier output must be 2 V p-p (into 150 Ω), requiring an amplifier gain (U1) of 2 times.

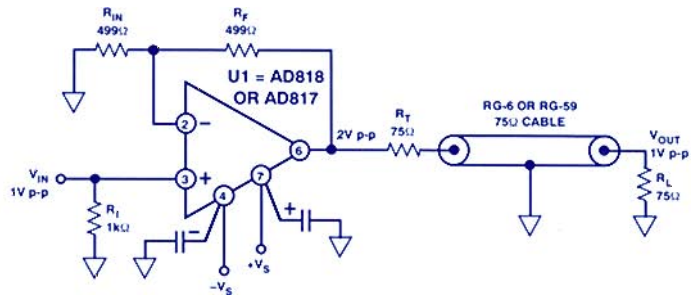


Figure 9. Impedance-matched line driver with 75- Ω load.

These systems have the advantage of wide bandwidth, but the low load impedances may require considerable power for high output levels—twice as much as appears at the load. Also, U1 must have a slew rate $2\times$ that required at the load. Nevertheless, for low signal levels (say, ≤ 2 V p-p), this drive system is quite practical, achieving high performance for a well-chosen U1, such as the AD818 or the AD817 (more below).

LINE DRIVER/RECEIVER CIRCUITS FOR VIDEO

Video Line Receivers

In high-speed communications, the line-receiver stage accepts video information from an incoming transmission line, and buffers it for local processing. Figure 10 shows a typical system to accomplish this, a single-ended driver at the input end of the coaxial transmission line—and a differential-input receiver. In principle, a differential end-to-end transmission system would be best, but single-ended drive systems are covered here because of their predominance. As the diagram shows, noise between driver/receiver grounds A and B is rejected by the inherently high common-mode rejection (CMR) of the differential video receiver.

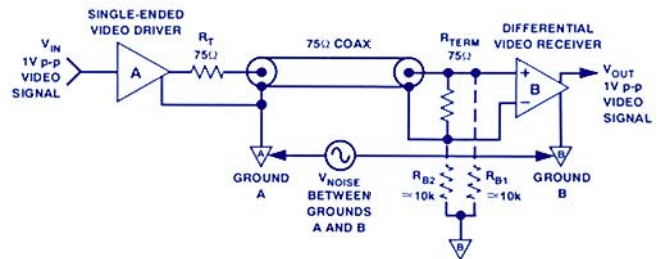


Figure 10. Video signal transmission system.

The coaxial line is terminated in its characteristic impedance by R_{TERM} , in this case 75 Ω . Because neither end of R_{TERM} is connected directly to ground B, both inputs of receiver B see essentially the same common-mode voltage, V_{NOISE} , which is rejected in proportion to B's CMR. A typical CMR goal is 70 dB or better for frequencies up to 10 MHz. Return resistors, R_{b1} and R_{b2} , if needed, keep I_{bias} from developing excessive CMV.

At V_{OUT} , stage B delivers a replica of the original driving signal V_{IN} . It may also amplify or attenuate the received signal and drive

an additional 75-Ω line. With proper terminations at both ends, these ideas also apply for line impedances other than 75 Ω.

Other critical parameters for this video receiver are signal bandwidth—for both the -3-dB and 0.1-dB frequencies (the latter is a typical HDTV requirement)—and video-distortion specifications. Video distortion is usually rated in terms of *differential gain* (%) and *differential phase* (°), while operating at rated load with 3.58- (NTSC) or 4.43-MHz (PAL) subcarriers.

Differencing-Op-Amp Line Receiver

Figure 11 shows a low cost, medium-performance video line receiver, using a high speed “video” op amp in a standard 4-resistor-bridge instrumentation amplifier. It is implemented for video with a high-speed, high-CMR op amp and low-resistance ac-trimmed resistors. Resistor matching is critical to CMR; for highest noise rejection, a single-substrate dual-matched-pair thin-film network should be used. Matching of the ratios, R_1/R_2 and R_3/R_4 , to 1% gives a low-frequency CMR of 46 dB. Above 1 MHz, the bridge balance is dominated by ac effects, and the $C_1 - C_2$ capacitive balance should be trimmed for best performance—a match that is essential for achieving CMR above 40 dB at high frequencies.

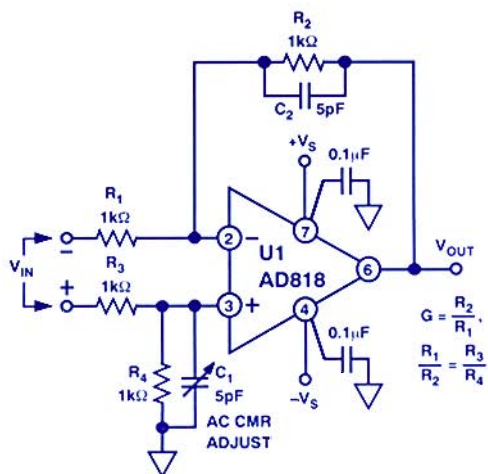


Figure 11. Simple video line receiver.

Video gain/phase performance of this stage depends on the choice of device for U1, the operating supply voltages, and the loading. Suitable amplifiers work best at supplies of ± 15 V, and with loads of 1 kΩ or more, since this maximizes the bandwidth of the op amp and minimizes loading. The AD817 and AD818* are the best all-around performers, capable of differential gain/phase of less than 0.1%/0.1°.

This circuit, with its two 1-kΩ input resistors, does load a 75-Ω video line somewhat; this loading should be taken into account.

Integrated Video Line-Receiver

Full integration of the video line-receiver eliminates drawbacks of the simple line-receiver approach and improves both performance and circuit flexibility. The AD830,† shown in Figure 12, is a two-input IC “active feedback amplifier” designed for this function.

The AD830 operates with supplies from ± 5 V to ± 15 V, has a 50-MHz bandwidth and a SR of 250 V/μs. Its two high-CMR, fully differential inputs handle signals up to ± 2 V. The current outputs of the input transconductance stages are summed and integrated via capacitor C; an output follower buffers its voltage.

In normal use, the input is connected to one differential pair; feedback is taken from the single-ended output and applied to the

other differential pair. Since the integrator seeks a steady state with its two input currents in balance, the feedback forces the output voltage, V_2 , to equal the input, V_1 . Since the common-mode rejection of this device is provided by the two inherently balanced differential input pairs, there is no need for matched resistor bridges, with their ac-trim and other problems.

In this basic application, the input signal is applied to input 1, and the output signal is tied to input 2. V_{OUT} is made equal to V_{IN} , while grounds, A and B, are isolated by the CMR of the AD830—typically 75 dB at frequencies below 1 MHz, 60 dB at 4.43 MHz, and essentially independent of supply voltage.

With only minor changes, a video line receiver with gain of 2 V/V can be implemented, simply by attenuating the feedback. Here, a pair of 499-Ω resistors, R_1 and R_2 , provide 2/1 attenuation. The gain expression is then similar to that for a non-inverting op-amp, $(1 + R_1/R_2)$. For lowest dc offset, use bias-balance resistor, R_3 , equal to $R_1 || R_2$.

As a ground-isolating video repeater, this circuit can drive a terminated 75-Ω output line, delivering a video output, V_{OUT} , equal to the original input, V_{IN} . Video distortion as a terminated-line driver is lowest for supply voltages $\geq \pm 10$ V; differential gain is typically 0.06%, and differential phase is about 0.08°. Gain- and phase errors are about double at ± 5 V.

VIDEO LINE DRIVERS

Video line-drivers buffer a signal from a single-ended board-level (possibly high-impedance) source, scale it if necessary, and drive an outgoing matched transmission line. The circuits that follow flesh out the terminated video transmission system (Figures 9 and 10) as to IC choices, operating options, and performance in “bread and butter” video applications. The circuit environment supplied allows a direct performance assessment.

A Workable Video Line Driver

The basic video line driver of Figure 13 uses the AD818, a low-cost amplifier noted earlier; it is capable of performing very well. The U1 stage gain is set at 2× by equal R_F and R_{IN} ; their resistance is low to minimize the feedback time-constant. The AD818 is compensated for stable operation at $G = 2$, with maxi-

*Use the reply card for technical data on these new products. Circle 6

†Use the reply card for technical data on this new product. Circle 7

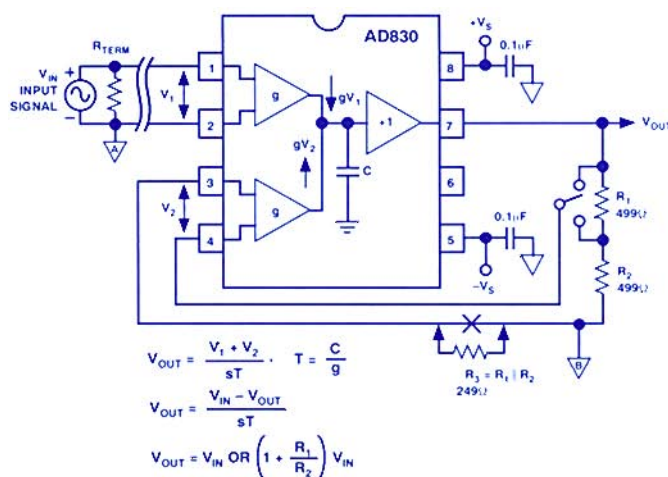


Figure 12. Improved video line-receiver architecture with AD830 differential feedback amplifier.

imum bandwidth of over 50 MHz. Since it doesn't use internal capacitive load compensation, it is quite linear.

The AD818's exceptional video differential gain and phase for an NTSC system are summarized in the figure for supplies of ± 5 V and ± 15 V. (The 150- Ω load represents the 75- Ω cable-drive system.) To minimize video distortion, loading should be minimized and maximum supply voltages used when possible. This circuit draws a power-conserving quiescent current of 6 mA. Other video-speed op amps can also be used for U1, with some increase of distortion. At ± 15 V, for example, the AD817 has typical gain/phase of 0.04%/0.08°.

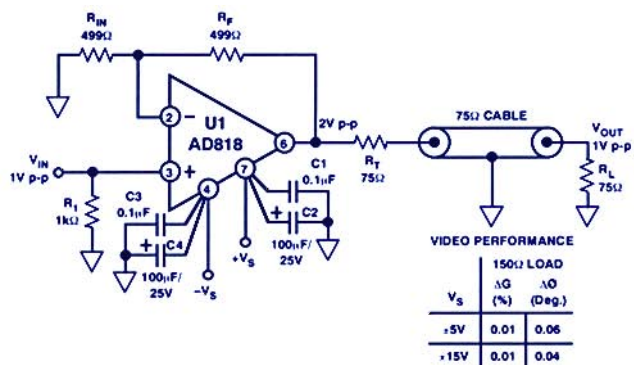


Figure 13. Basic (good) video line driver.

A Higher Performance Video Driver

Figure 14 shows a higher-performance video line driver using the AD810 transimpedance amplifier. This circuit is also relatively inexpensive, but it can perform better than Figure 13 because of the AD810's appreciably higher SR and gain-bandwidth, plus its higher output current. It also has an optional DISABLE function; the stage can be shut down by control logic.

The differential gain and phase of the AD810 are summarized in the figure for supplies of ± 5 V and ± 15 V. As with the AD818 circuit, NTSC video distortion is low, at 0.03%/0.05°, with minimal loading and high supply voltage. However, the AD810 also does relatively well with ± 5 -V supplies; it is the amplifier of choice for such configurations. Like the AD818, the AD810 has a low quiescent current, 8 mA.

The AD810 has a -3-dB bandwidth of 65 MHz here, and a ripple-free 0.1-dB bandwidth of 20 MHz, both better than for Figure 14. The DISABLE pin (8) is active-low to shut the device down to a standby current drain of 2 mA, with 60-dB input-output isolation at 10 MHz. This permits on/off logic control of a single IC—or multiplexing the outputs of a number of devices.

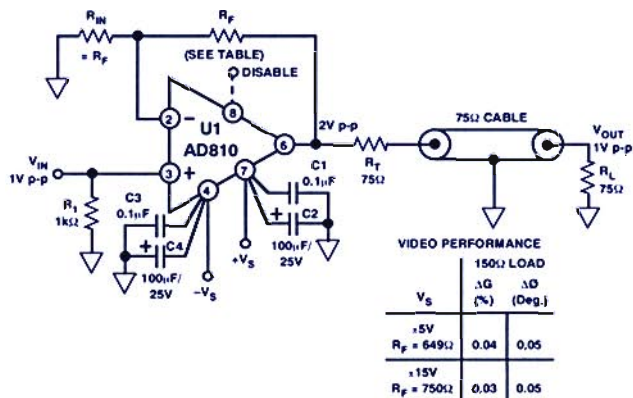


Figure 14. High-performance (better) line driver.

The AD810, a transimpedance amplifier, *must* be used with the correct value of R_F for best results. The figure indicates the different values, optimized for bandwidth, for ± 5 V and ± 15 V.

Highest Performance Video Driver/Distribution Amp

Figure 15 illustrates a very high performance video line driver. This circuit uses the AD811§ as a gain-of-2 video buffer or line driver. It differs from the driver circuits of Figures 13 and 14 in that it optionally doubles as a distribution amplifier, driving two output lines. Operating at a gain of 2, the AD811 drives a pair of 75- Ω output lines through 75- Ω terminations. V_{OUT1} and V_{OUT2} are individually isolated/buffered replicas of V_{IN} .

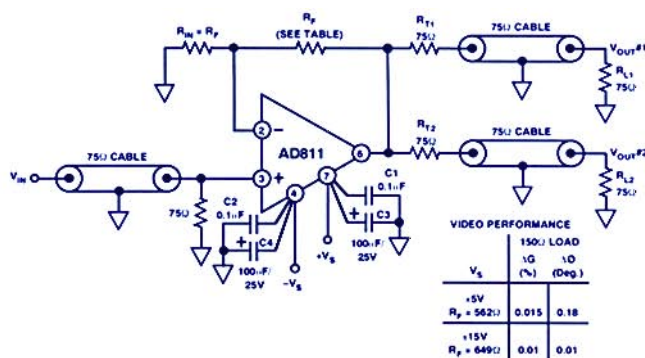


Figure 15. Higher-performance (even better) line driver/distribution amplifier.

With ± 15 -V supplies, the circuit's -3-dB bandwidth is 120 MHz, with NTSC differential gain/phase of 0.01%/0.01° driving one line ($R_L = 150 \Omega$). The gain flatness (ripple free) is within 0.1 dB to 35 MHz. For two lines, the gain errors are about the same, but the phase errors increase to 0.04°.

Though lower supply voltage degrades performance, differential phase is still $< 0.18^\circ$ with ± 5 V. The -3-dB frequency drops to 80 MHz, and 0.1-dB gain flatness is held to 25 MHz. Full video capability is achieved for supply voltages $> \pm 10$ V. ■

§Use the reply card for technical data on this new product. Circle 6

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Decreasing Size, More-Demanding Performance Pace Disk-Drive IC Design

Read-channel and servoloop IC subsystems provide increasing integration

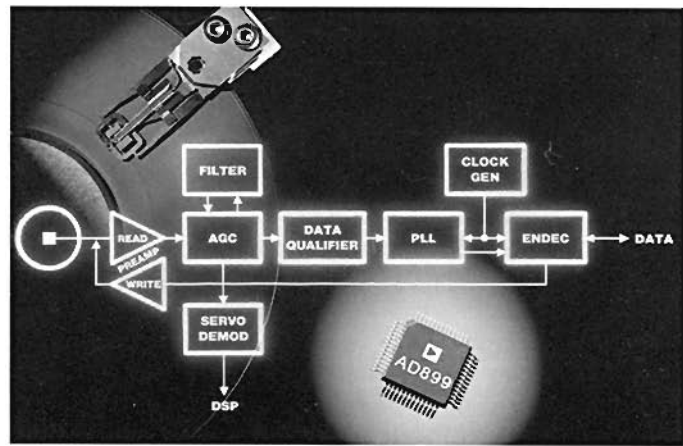
by Bill Schweber

Hard-disk drives (HDDs) are extremely sophisticated, highly integrated electromechanical designs. For years they have been trending toward ever-smaller size, calling for a continuing procession of new generations of high-performance components—mechanical structures, transducers, integrated-circuit ICs, and other electronic components. Key challenges are posed by the speed and precision required for head positioning—and in the *read* channel's need to provide error-free interpretation of data picked up by the *read* head. Analog Devices now provides a new generation of carefully tailored special-purpose monolithic linear ICs to ease the challenge to the designer for the *read* channel and for the servo-control path.

READ CHANNEL: THE AD899

The new-generation integrated *read*-system chip, the AD899*, incorporates more of the necessary functions onto a single device than its predecessors (the AD890 & AD891—*Analog Dialogue* 22-1—and the AD897—25-2). This sophisticated IC (Figure 1) incorporates all *read*-channel functions into a single device—except for the head preamplifier, which is mounted at the head to maximize achievable signal-to-noise ratio. Integrated on the chip are signal conditioning, data qualification, data synchronization, servo demodulation, and data encoding/decoding (RLL 1,7 format and others). A minimum of external components are required.

The AD899 design also includes the essential *write* functions, which are relatively easy to implement. An input clamp provides read-after-write overdrive protection, to minimize front-end recovery time after the relatively large *write* pulse to the head.



Write precompensation is also incorporated, to anticipate distortion of the pulse shapes in the time domain and reduce intersymbol interference (ISI).

To process the raw analog signal from the *read* head into a valid, timed digital signal representing bits of information from the disk, the AD899 includes:

- automatic gain-control (AGC)
- filters
- two levels of data qualification
- data synchronizer
- encoder/decoder (endec)
- *write*-clock synthesizer
- servo demodulator

The programmable filter approximates a seventh-order Bessel function. It is designed to provide both a low-pass-filtered and a differentiated output at the same time, without an intervening time delay. This is important for the data-qualification scheme, which depends on time-coherency between the low-pass output and its differentiated version.

All this is done at a continuous rate of from 6.67 to 32 megabits/second, compatible with the high transfer-rate requirements of today's drive systems.

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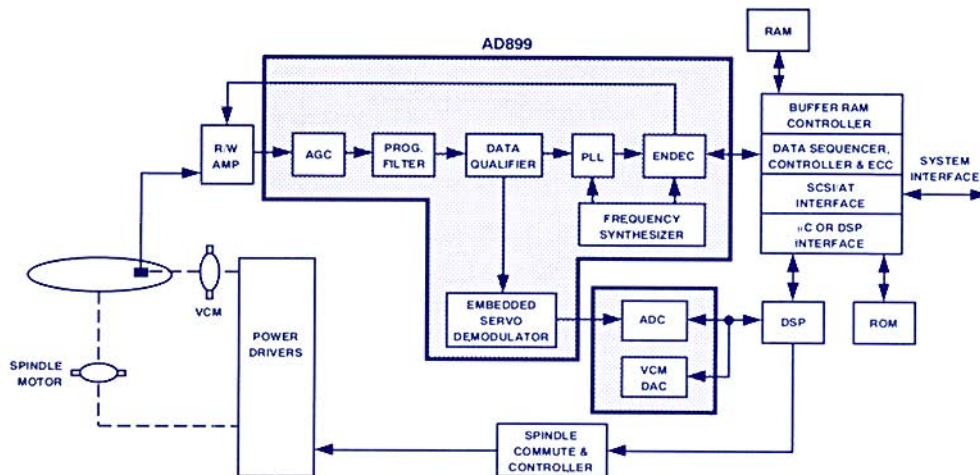


Figure 1. Block diagram of hard-disk drive electronics.

The device is controlled via a serial port. All major read-channel characteristics are programmable, including AGC setting, filter cut-off frequency and boost, data-qualification amplitude threshold, data-synchronizer center frequency and window center, *write*-precompensation setting (both early and late), and M and N (major and minor) divider ratios for the frequency synthesizer.

Data-bit qualification Starting with the head, the various blocks of the *read* channel treat the signal in cascade. The AGC and filtering seek to maintain constant signal level (despite wide variations in the signal received from the head due to electronic and mechanical causes), to filter noise, and to shape the *read* pulse. The leveled, shaped pulses must then be *qualified*, or judged as to whether they are artifacts or constitute valid bit information, to achieve minimum bit error rate (BER) at the high transfer rate.

The AD899 is housed in a 52-pin quad flat-pack and requires a single +5-V supply. Although nominal power consumption is 0.75 W, the device's six major subsections (AGC/filter, servo demodulator, endec, data qualifier, data synchronizer, and frequency synthesizer) can be selectively powered-down. It is priced at less than \$10 in OEM quantities.

SERVOLOOP: THE AD7773 AND AD7775

The AD7773 and AD7775 embedded-servo front-end chips* are fully integrated burst demodulators used to capture the sequential servo bursts which are recorded at the beginning of each servo sector on the disk. They provide the functions needed to implement the servo demodulation and head positioning in the servo

system, in order to step the head assembly smoothly to the desired track and keep the head properly centered over this track.

Each (Figure 2) contains a 10-bit, 3- μ s A/D converter; two D/A converters with output amplifiers (10-bit, 4- μ s settling time and 8-bit, 3- μ s settling); a burst demodulator, and processor interface. Identical in all other respects, the devices differ only in the processor interface: the AD7773 has a 10-bit data port with separate address pins, while the AD7775 has a multiplexed address/data bus with an address-latch-enable (ALE) control signal.

For the input channel, the demodulator captures high speed servo data, consisting of a variety of embedded patterns. Up to four sequential servo burst signals can be synchronously demodulated, full-wave rectified, and integrated. The integration technique used here offers improved channel SNR, in contrast to the peak-detection technique used by most available designs. At the end of the burst period, the integrated output voltage (representing the amplitude of a captured burst) is sampled and held on one of four internal track/hold amplifiers—ready for digitizing. After conversion, the results are fed to four 10-bit-wide on-chip data registers.

For control, the 10-bit D/A converter's output (DAC A) controls the head position via the voice-coil motor. The 8-bit D/A converter's output (DAC B) is available for control of spindle speed, gain, or filter, or any auxiliary purpose.

Demodulator channel operation The demodulator channel (Figure 3) can operate in either of two major modes: synchronous detection and gated detection. In synchronous mode, a zero-crossing detector synchronously detects full cycles of the input signal, which are then rectified and integrated. The number of cycles within a burst and the number of bursts to be captured are both programmable.

In the gated detector mode, the synchronous detector is bypassed and the input is simply rectified and integrated. A third mode, calibration, allows a reference signal to be applied as input for measuring any mismatch among the four track/hold amplifiers.

The AD7773 and AD7775, packaged in a 28-pin SOIC, require a single +5-V supply; they support a power-down mode which turns off all linear circuitry. Price is \$14.50 (1000s).

The AD899 was designed by a team at our Analog Signal Processing group, Wilmington, MA; the AD7773 and AD7775 were designed in our Converter group at Analog Devices BV, Limerick, Ireland.

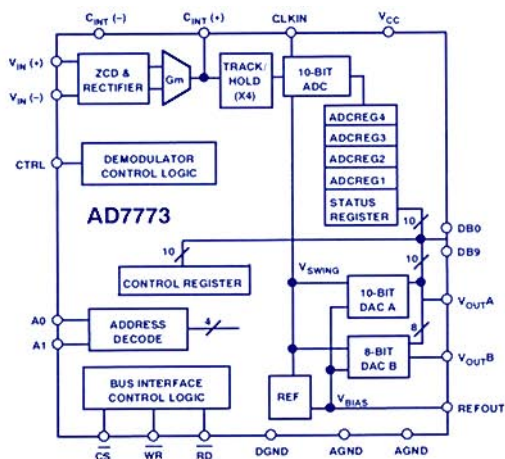


Figure 2. Block diagram of AD7773 embedded servo front end.

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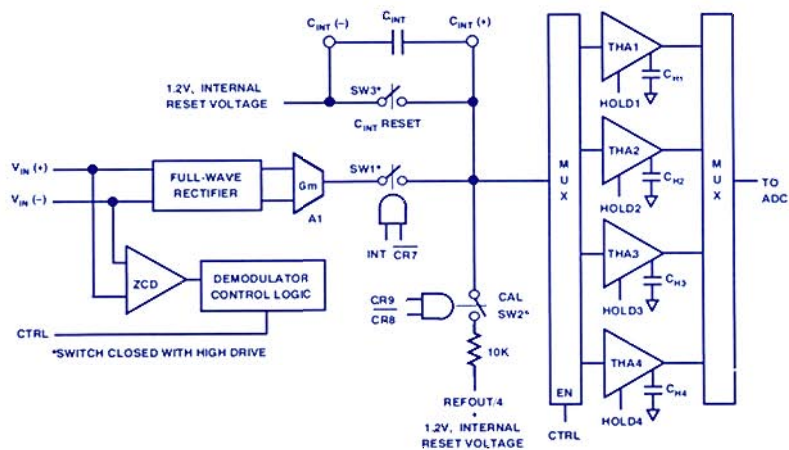


Figure 3. Demodulator channel block diagram.

Low-Cost 12-Bit IC Resolver-to-Digital Converter Emulates Optical Encoder

Complete AD2S90 has absolute-angular-position serial binary and 1024-line incremental-encoder A quad B output formats

The AD2S90* is a 12-bit monolithic resolver-to-digital converter. A successor to the AD2S81—the first 12-bit monolithic R/D converter, introduced in these pages in 1987 (*Analog Dialogue* 21-1, pp. 23-24)—the AD2S90 is complete and requires no external components for operation.

The AD2S90 makes available two forms of digital output data. The first, serial 12-bit binary, gives absolute angular position without requiring a large number of pin contacts; this permits the device to be housed in a small, low-cost package. The second is a pair of incremental pulse outputs, which emulate the A quad B output of a 1024-line incremental optical rotary encoder with selectable North-marker width; this compatible format permits the AD2S90, combined with a rugged, reliable resolver, to interface with digital control systems designed for optical encoders. It also confers the benefits of redundancy, since the absolute output can be read at any time to check on the accuracy of (and update) the accumulated encoder count.

In addition to the digital output, the AD2S90 also makes available an analog voltage proportional to velocity (nominally ± 150 rps/V); it can be used in control loops as a derivative feedback to improve speed and stability.

The AD2S90 is useful wherever the need exists for digital angular information for measurement and control. Typical places where it might be used are in industrial motor control, servo controls, industrial gauging, automotive motion sensing and control, robotics, and factory automation.

A REVIEW OF PRINCIPLES

As the block diagram indicates, the AD2S90 employs a tracking loop. The three inputs to the chip, with a nominal range of 2 V rms, at frequencies from 3 to 20 kHz, are the resolver's ac reference signal and its two quadrature outputs (*sin* and *cos*). The chip multiplies the quadrature inputs with the sine of the digital output angle, computing an ac voltage proportional to the sine of the angular difference (error).

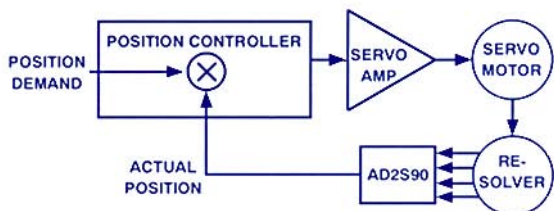


Figure 1. Position-control loop.

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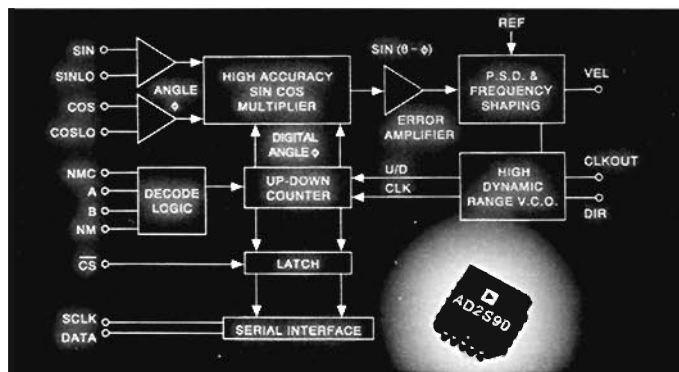


Figure 2. Motion-control loop using the AD2S90.

The ac voltage is demodulated by a phase-sensitive detector (PSD), integrated, and applied to a voltage-controlled oscillator (VCO). The oscillator output causes a counter to increment the digital output angle until the angular difference is zero, and to track the input angle by counting up or down to correct an error whenever the input to the VCO is non-zero. As a type II tracking loop, it also tracks continuously to maintain velocity error at zero.

Because the count rate is proportional to the VCO input, the VCO input voltage provides an analog measure of angular velocity. Also, since the pulse train from the VCO is integrated by a counter to produce a digital angle, it is basically of the same form as the train of pulses from an incremental optical encoder. The AD2S90 forms these pulses into two orthogonal streams to fit the A quad B format, and provides both a direction (DIR) signal and a North marker (NM) with three selectable widths—as an absolute position reference. When the 1024-line encoder signals are decoded, they produce 12-bit information.

Several AD2S90s can be easily multiplexed on a serial data line, a handy feature when multi-axis position information is desired. A given unit's output is read only when its chip-select line (\overline{CS}) is brought low.

The converter has a bandwidth of 1 kHz; the maximum tracking rate is 375 rps at 12-bit resolution. A single accuracy grade is available, the AD2S90AP. Housed in a 20-pin PLCC, specified for the 40 to +85°C temperature range, it requires only 50 mW of operating power at ± 5 V. It is priced at just \$25 in 1000s.

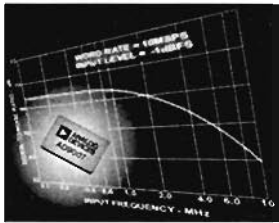
APPLICATIONS

The AD2S90 is useful in position and motion control. Figure 1, a block diagram of a rudimentary position followup system, shows where an AD2S90 would be used. In Figure 2, the AD2S90 is shown in an adaptation to a control system calling for incremental position inputs. The serial absolute position is available as a "reality check", and the velocity output is available as an optional feedback. The AD2S90 can be readily used with a variety of digital signal processors, including the ADSP-2105. ▶

10-MSPS ADC

12-bit low-cost AD9007

Low power at +5, -5.2 V

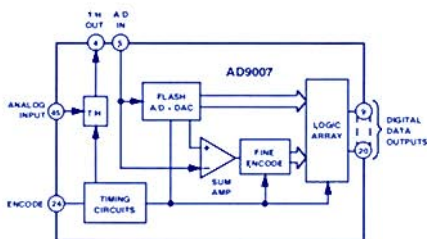


The AD9007* is a complete 12-bit sampling A/D converter specified to operate at sampling rates up to 10 MSPS. TTL-compatible, with parallel twos-complement outputs, it is housed in a 46-pin hermetic metal DIP. Typical application areas include radar, digital radio, and medical scanners.

Employing proprietary monolithic circuits and process technologies, this hybrid-function-compatible with ADC603/604-type 12-bit, 10-MSPS devices—needs only +5 and -5.2-volt supplies, consumes only 3.6 watts, and is specified for operation over the full -25 to +85°C temperature range. It is available in two grades (A/B). Prices (100s) start at \$420/\$504.

Functionally complete, the device includes track-and-hold circuitry, an analog reference, and all timing circuits. It accepts inputs in the range of ±1.25 V and guarantees no missing codes over the full temperature range.

Dynamic performance specs include an analog -3-dB bandwidth of 150 MHz—useful in undersampling applications. For B-grade units, with input 1 dB below full scale at +25°C, minimum signal-to-noise ratio (including harmonics) for 0.1, 2.3, and 4.3 MHz is 67, 66, and 65 dB; and max in-band harmonic distortion component at the same frequencies is -80, -77, and -75 dBc. Intermodulation distortion (two-tone, 2.2 & 2.3 MHz) is typically -81dBc. ■



*Use the reply card for data. Circle 17

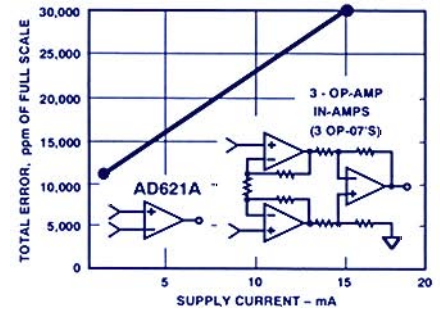
In-Amp Features Low Drift & Cost

AD621 has excellent dc & ac specs, low noise, low dissipation, wide power-supply-voltage range

The AD621† Instrumentation Amplifier is a high-performance gain block with total error specified as a system at pin-programmable fixed gains of 10 and 100. The lowest-cost alternative to three-amplifier-plus-precision-resistor home-grown designs, it is available in a choice of 8-pin plastic mini-DIP, cerdip, and SOIC packages.

With its low noise, the lowest total drift (offset plus gain) of any in amp, excellent ac specifications, low supply current, and wide supply-voltage range, it offers an optimum performance mix for weigh scales, sensor interfacing and data-acquisition, industrial process controls, and battery-powered and portable equipment. Prices (A/B grades, mini-DIP) start at \$3.82/\$5.74 in 1000s.

With gain of 100, noise spectral density, referred to the input, is typically 9 nV/√Hz at 1 kHz, with 0.28 μV p-p for the 0.1-10-Hz band. Offset (B grade) is 50 μV max at 25°C, 215 μV max over temperature (0.6 μV/°C max), with max bias current



of 1.5 nA over temperature, and gain error & drift of 0.05% & 5 ppm/°C. Max non-linearity is 10 ppm FS (all grades).

Common-mode rejection (B) is 120 dB min at 60 Hz, with 1-kΩ source unbalance (gain of 100); bandwidth is 200 kHz (-3-dB), with typical slew rate and settling time of 1.2 V/μs and 12 μs. The AD621 draws 1.3-mA max supply current and will operate on supplies from ±2.3 V to ±18 V. An output reference terminal permits the output to be offset or connected to system ground. ■

†Use the reply card for technical data. Circle 18

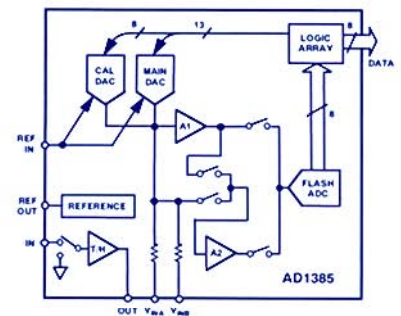
16-Bit, 500-kSPS Sampling ADC

AD1385 is complete, includes autozeroing and automatic digital calibration for linearity

The AD1385§ is a complete 16-bit, 500-kSPS sampling A/D converter, housed in a single hybrid package. It includes a track-hold amplifier, subranging ADC, voltage reference, autozeroing, and calibration for linearity. Its excellent ac specifications make it suitable for applications that call for high spectral purity, such as MRI and radar.

The linearity calibration cycle, completed within 15 ms, digitally compensates for differential nonlinearity and internal component mismatches, as well as other parametric shifts over the (user-selectable) ±5 or ±10-volt input ranges and case temperatures from -55 to +125°C. Autozeroing upon demand nulls internal offsets in the track-hold amplifier and the ADC.

THD and SNR are 90 dB min for a 5-kHz input signal; at 200 kHz, SNR is still 88 dB, useful for DSOs and spectrum ana-



lyzers. With differential and integral non-linearity of ±0.0006% and 0.0015% FSR, and no-missing codes to 16 bits, its dc precision is suitable for measurement & test and CAT scanners.

The AD1385 requires ±5-V and ±15-V power supplies and an external 10-MHz clock for 500-kSPS operation. Output data are multiplexed in two bytes onto an 8-bit data bus. Pricing starts at \$687 in 100s. ■

§Use the reply card. Circle 19

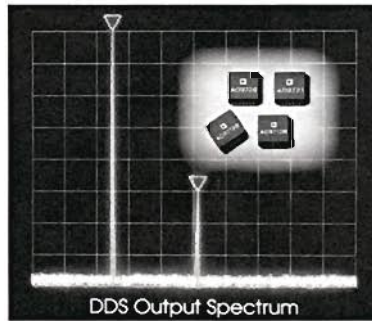
Four High-Speed DACs for DDS

10-bit AD9720/9721: 400 (ECL)/100 (TTL) MSPS

12-bit AD9712B/9713B: 100 (ECL)/80 (TTL) MSPS

Four of the industry's fastest DACs designed for direct digital synthesis (DDS), waveform reconstruction, and high-resolution video applications are now available from Analog Devices. The 10-bit AD9720 and AD9721* work in ECL-compatible 400-MSPS and TTL-compatible 100-MSPS applications, while the 12-bit AD9712B and AD9713B†, improved versions of earlier designs (*Analog Dialogue* 23-4 (1989) p. 6) are for 100-MSPS (ECL) and 80-MSPS (TTL).

The monolithic devices, constructed in an oxide-isolated bipolar process, are available in SOICs, plastic DIPs, cerdips, and LCCs. The AD9720/21 are available in two grades, B for -25 to +85°C, and T, for -55 to +125°C. The AD9712B/13B are available in A, B (industrial), and S, T (military) grades. The AD9713B and AD9721 were designed to operate with the AD9955 100-MHz direct digital synthesizer.



The table compares the specs of B-grade devices (-25 to +85°C):

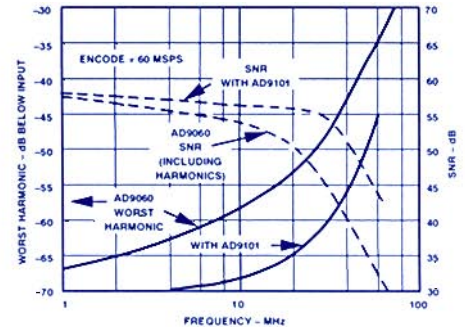
Characteristic	Devices:	AD9720	AD9721	AD9712B	AD9713B
Resolution (bits)		10	10	12	12
Update rate, min (MSPS)		400	100	100	80
Diff. nonlin., max (LSBs)		0.75	0.75	0.75	0.75
Int. nonlin., max (LSBs)		1.0	1.0	1.0	1.0
COIT (pF)		6	6	15	15
Settling time, 1/2 LSB (ns)		4.5	4.5	27 (1 LSB)	27 (1 LSB)
Glitch impulse (pV-s)		1.5	1.5	28	28
Setup time, min over T (ns)		1.2	1.2	0.8	0.8
Hold time, min over T (ns)		2.0	2.3	2.0	2.0
SFDR (200 Hz span), dBc		75	75	72	72
Price, starting \$US (100s)		\$79	\$40	\$65	\$65

*Circle 20 for 10 bits, †Circle 21 for 12 bits

125-MSPS S/H

AD9101: 8-bit-accuracy

12-bits @ 50 MSPS



The AD9101 Sampler™, an ultrafast high-performance monolithic sampling amplifier,† can be clocked at up to 125 MSPS, with a sampling bandwidth of 350 MHz. It consists of an innovative track-and-hold circuit and a gain-of-4 amplifier; it is available in SOIC and ceramic LCC packages.

In the *track* mode, it has a typical 7-ns acquisition time to 0.1%, with 14 ns maximum to 0.01%. A low-noise device, it has noise spectral density of 3.3 nV/√Hz at 10 MHz. Switching to *hold*, aperture jitter is typically less than 1 ps rms, and pedestal offset is ±20 mV max. In *hold*, feedthrough rejection is 66 dB at 50 MHz, and the worst harmonic is typically -57 dB, sampled at 125 MSPS.

Fast and accurate, it has many potential applications. It can improve the performance of flash converters (as shown above); and it can be used in deglitching D/A converters for direct digital synthesis. Further applications exist in directly sampling IF signals in digital radio, HDTV cameras, digital sampling oscilloscopes, peak detectors, spectrum analyzers, and test equipment.

Two temperature/performance grades are available, A, -40 to +85°C, packaged in 20-pin SOIC and 20-contact ceramic LCC, and S, for -55 to +125°C, packaged in the ceramic LCC. Both grades have comparable performance specifications at +25°C and over their respective temperature ranges—but the worst harmonic, over temperature, for a 48-MHz signal, sampled at 100 MSPS, is -53 dBFS for A and -51 dBFS for S. Prices in 100s start at \$33. □

Use the reply card for technical data. Circle 23

32-Bit Floating-Point DSP @ \$49.90

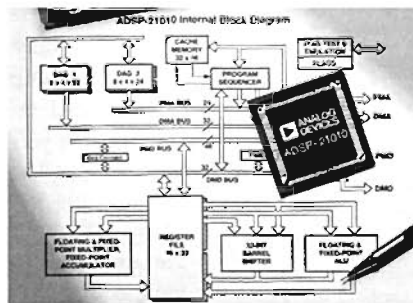
Performs complex 1024-point FFT in 1.54 ms

ADSP-21010: has powerful low-cost tool support

The ADSP-21010‡ is a 32-bit floating-point digital signal-processor (DSP) based on the architecture of the popular ADSP-21020, (*Analog Dialogue* 25-2, p. 3). Apart from the low cost of the chip itself, the IC is supported by powerful low-cost tools, making the "total cost of DSP entry" far less than for other solutions available today.

The ADSP-21010 can perform a complex 1024-point FFT in 1.54 milliseconds at a 12.5-MHz instruction rate (80 ns per cycle), using external memory. This is more than twice as fast as a major competitive device, using a 60-ns cycle time; the ADSP-21010's longer cycle time permits the use of slower, lower-cost memory chips.

Available low-cost tools include EZ-KIT™, which comprises development software, assembler, and simulator, plus the EZ-LAB™ Evaluation Board. A low-cost development package with C compiler and emulator will be available soon.



The ADSP-21010 supports 32-bit IEEE floating-point and fixed-point operations, (the ADSP-21020 also supports IEEE 40-bit floating-point operations) and attains a 0.77-ms FFT benchmark, with its 40-ns cycle time. The devices are source- and object-code compatible. Since both use the same package, a 304-pin PQFP, designs using the lower-cost unit can migrate upward. Price of the ADSP-21010 is \$49.50 in 100s, and of the EZ-KIT is \$1495. □

‡Use the reply card. Circle 22

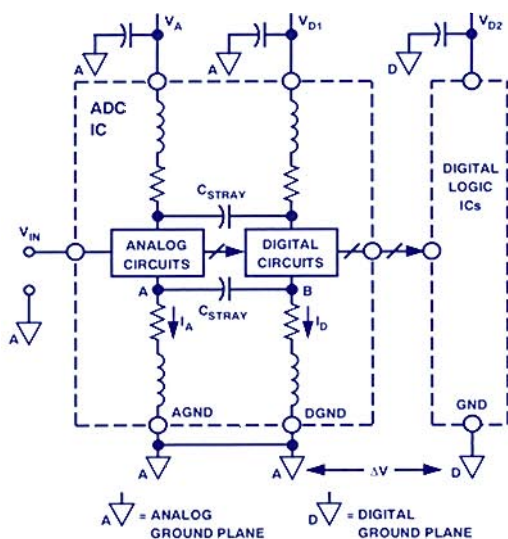
GROUNDING (AGAIN)

by Walt Kester

Q. *I've read your data sheets and application notes and also attended your seminars, but I'm still confused about how to deal with analog (AGND) and digital (DGND) ground pins on an ADC. Your data sheets usually say to tie the analog and digital grounds together at the device, but I don't want the ADC to become my system's star ground point. What do I do?*

A. First of all, don't feel bad that you are confused about what to do with your analog and digital grounds. So are lots of folks! Much of the confusion comes from the labeling of the ADC ground pins in the first place. The pin names, AGND and DGND, refer to what's going on inside the component itself and do not necessarily imply what you should do with them externally. Let me explain.

Inside an IC that has both analog and digital circuits, such as an ADC, the grounds are usually kept separate to avoid coupling digital signals into the analog circuits. The diagram shows a simple model of an ADC. There is really nothing the IC designer can do about the wirebond inductance and resistance associated with connecting the pads on the chip to the package pins. The rapidly changing digital currents produce a voltage at point B which will inevitably couple into point A of the analog circuits through the stray capacitance. It's the IC designer's job to make the chip work in spite of this. However, you can see that in order to prevent further coupling, the AGND and DGND pins should be joined together externally to the same low impedance ground plane with minimum lead lengths. Any extra external impedance in the DGND connection will cause more digital noise to be developed at point B; it will, in turn, couple more digital noise into the analog circuit through the stray capacitance. Though an extremely simple model, this serves to illustrate the point.



Q. *O.K., you've told me to join the AGND and DGND pins of the IC together to the same ground plane—but I am maintaining separate analog and digital ground planes in my system. I want them tied together only at one point: the common point where the power supply returns are all joined together and connected to chassis ground. Now what do I do?*

A. If you have only one data converter in your system, you could actually do what the data sheet says and tie your analog and digital ground systems together at the converter. Your system star ground point is now at the data converter. But this may be extremely undesirable, unless you initially planned your system with this thought in mind. If you have several data converters located on different PCBs, the concept breaks down, because the analog and digital ground systems are joined at each converter on a number of PCBs. This is a perfect invitation for ground loops!

Q. *I think I've figured it out! If I must join the AGND and DGND pins together at the device, and I want to maintain separate system analog and digital grounds, I tie both AGND and DGND to either the analog ground plane or the digital ground plane on the PCB, but not both. Right? Now, which one should it be, since the ADC is both an analog and a digital device?*

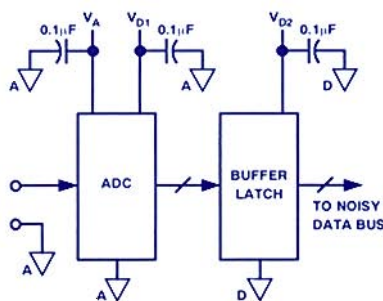
A. Correct! Now, if you connect the AGND and DGND pins both to the digital ground plane, your analog input signal is going to have digital noise summed with it, because it is probably single-ended and referenced to the analog ground plane.

Q. *So the right answer is to connect both AGND and DGND pins to the analog ground plane? But doesn't this inject digital noise on my nice quiet analog ground plane? And isn't the noise margin of the output logic degraded because it now referenced to the analog ground plane, and all the other logic is referenced to the digital ground plane? I plan to run the ADC outputs to a backplane tristate data bus which is going to be pretty noisy to begin with so I think I need all the noise margin I can get.*

A. Well, nobody ever said life was easy or fair! You have reached the right conclusion by traveling a rocky road, but the problems you suggest—digital noise on your analog ground plane and reduced noise margin on your ADC outputs—really aren't as bad as they seem; they can be overcome. It is clearly better to let a few hundred millivolts corrupt the digital interface than to apply the same corrupting signal to the analog input where the least-significant-bit for a 16-bit, 10-V-input-range ADC is only 150 μV ! First of all, the digital ground currents on DGND pins can't really be that bad, or they would have degraded the internal analog parts of the ADC in the first place! If you bypass the power pins of the ADC to the analog ground plane, using a good-quality high-frequency ceramic capacitor for high frequency noise (say 0.1 μF), you will isolate these currents to a very small region around the IC, and they will have minimal effect on the rest of your system.

You will incur some reduction in digital noise margin, but it is usually acceptable with TTL or CMOS logic if it's less than a few hundred millivolts or so. If your ADC has single-ended ECL outputs, you may want to put a push-pull gate on each digital output—i.e., one with both true and complementary outputs. Tie the grounds of this gate package to the analog ground plane and connect the logic signals differentially across the interface. Use a differential line receiver at the other end which is grounded to the digital ground plane. The noise between the analog and digital ground planes is now common-mode—most of it will be rejected at the output of the differential line receiver. You could use the same technique with TTL or CMOS, but there is usually enough noise margin not to require differential transmission techniques.

However, one thing you said troubles me greatly. In general, it is unwise to connect the ADC outputs directly to a noisy data bus. The bus noise may couple back into the ADC analog input through the stray internal capacitance—which may range from 0.1 to 0.5 pF. It is much better to connect the ADC outputs directly to an intermediate buffer latch located close to the ADC. The buffer latch is grounded to your digital ground plane, so its output logic levels are now compatible with those of the rest of your system.



Q. I think I understand now, but why on earth didn't you just call all the ground pins of your ADC AGND in the first place; then none of this would have come up in the first place?

A. Perhaps. But what if the incoming-inspection person connects an ohmmeter between these pins and finds out that they are not actually connected together inside the package? The whole lot will probably be rejected—and the IC may be blown! Furthermore, there is a tradition associated with ADC data sheets which says we must label the pins to indicate their true function, not what we would like them to be.

Q. O. K. Now, here comes a question I've been saving as your ultimate test! I have a colleague who designed a system with separate analog and digital ground systems. My colleague says that, with the ADC's AGND pin connected to the analog ground plane and the DGND pin connected to the digital ground plane, the system is working fine! How do you explain this?

A. First of all, just because a practice is not recommended doesn't necessarily mean you can't get away with it some of the time and thereby be lulled into a false sense of security. (This is one of the lesser-known of Murphy's Laws). Some ADCs are less sensitive to external noise between the AGND and DGND pins, and it may be that your colleague picked one of those by accident. There could be other explanations—which would require that we explore your colleague's definition of "working fine"—but the point is that the ADC's specifications are not guaranteed by the manufacturer under those operating conditions. With a complex component like an ADC, it is impossible to test the device under all possible operating circumstances, especially those which aren't recommended in the first place! Your friend got lucky this time, but you can be sure that Murphy's law will ultimately catch up with him (or her) if this practice is continued in future system designs.

Q. I think I understand the ADC grounding philosophy now, but what about DACs?

A. The same philosophy applies. The DAC's AGND and DGND pins should be tied together and connected to the analog ground plane. If the DAC has no input latches, the registers driving the DAC should be referenced and grounded to the

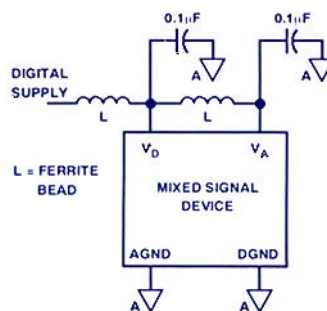
analog ground plane to prevent digital noise from coupling into the analog output.

Q. What about mixed-signal chips which contain ADCs, DACs, and DSPs such as your ADSP-21msp50 voiceband processor?

A. The same philosophy applies. You should never think of a complex mixed-signal chip, such as the ADSP-21msp50, as being only a digital chip! The same guidelines we've just been discussing should be applied. Even though the effective sampling rate of the 16-bit sigma-delta ADC and DAC is only 8 ksp/s, the converters operate at an oversampling frequency of 1 MHz. The device requires an external 13-MHz clock, and an internal 52-MHz processor clock is generated from it with a phase-locked loop. So you see, successful application of this device requires an understanding of design techniques for both precision- and high-speed circuits.

Q. What about the analog and digital power-supply requirements of these devices? Should I buy separate analog and digital power supplies or use the same supply?

A. This really depends on how much noise is on your digital supply. The ADSP-21msp50, for example, has separate pins for the +5-V analog supply and the +5-V digital supply. If you have a relatively quiet digital supply, you can probably get away with using it for the analog supply too. Be sure to properly decouple each supply pin at the device with a 0.1-µF ceramic capacitor. Remember to decouple to the analog ground plane, not the digital ground plane! You may also want to use ferrite beads for further isolation. The diagram below shows the proper arrangement. A much safer solution is to use a separate +5-V analog supply. You can generate the +5 V from a quiet +15-V or +12-V supply using a three-terminal regulator, if you can tolerate the extra power dissipation. ■



REFERENCES [not available from Analog Devices unless noted]

1. Ralph Morrison, *Grounding and Shielding Techniques in Instrumentation*, Third Edition. New York: Wiley-Interscience, 1986.
2. Henry W. Ott, *Noise Reduction Techniques in Electronic Systems*, Second Edition. New York: Wiley-Interscience, 1988.
3. *High-Speed Design Seminar*, 1990. Norwood MA: Analog Devices, Inc. Use book purchase card.
4. *Mixed-Signal Design Seminar*, 1991. Norwood MA: Analog Devices, Inc. Use book purchase card.
5. Paul Brokaw, "An I.C. Amplifier User's Guide to Decoupling, Grounding and Making Things Go Right for a Change." AN-202. Free from Analog Devices. Circle 24
6. Jeff Barrow, "Avoiding Ground Problems in High Speed Circuits," *R.F. Design*, July, 1989.
7. Paul Brokaw and Jeff Barrow, "Grounding for Low- and High-Frequency Circuits," *Analog Dialogue* 23-3, 1989. Free from Analog Devices. Circle 12
8. *The Best of Analog Dialogue—1967-1991*. Norwood MA: Analog Devices, Inc. Free from Analog Devices. Circle 13

by James Bryant

TIME REFERENCES (continued from 26-1-AA-11)

Q. *Why do you say that the clock of a system is a reference?*

A. This comment does not necessarily apply to the conversion clock of an ADC; it applies principally to the sampling clock of a sampled-data system. In these systems, the signal is required to be sampled repeatedly at predictable (usually equal) intervals for storage, communication, computational analysis, or other types of processing. The quality of the sampling clock is a system-performance-limiting factor.

Q. *But crystal oscillators are very stable, aren't they?*

A. They have good long-term stability, but they are often used in ways which introduce short-term phase noise. Phase noise is also introduced by designers who, instead of using crystal oscillators, use R-C relaxation oscillators (such as the 555 or the 4046)—which have a great deal of phase noise.

Q. *How can I ensure that my sampling clock has low phase noise?*

A. Don't use the crystal oscillator circuitry in your microprocessor or DSP processor as the source of your sampling clock. If at all possible, do not use a logic gate in a crystal oscillator. Crystal oscillators made with logic gates generally overdrive the crystal; this is bad for its long term stability, and usually introduces worse phase noise than would a simple transistor oscillator. In addition, digital noise from the processor—or from other gates in the package if a logic gate is used as an oscillator—will appear as phase noise on the oscillator output.

Ideally, use a single transistor or FET as your crystal oscillator and buffer it with a logic gate. This logic gate, and the oscillator itself, should have a well-decoupled supply; the other gates in the package should not be used because logic noise from them will phase-modulate the signal. (They may be used for dc applications but not for fast-switching operations.)

If there is a divider between the crystal oscillator and the sampling clock input of the various ADCs, the divider power supply should be decoupled separately from the system logic to keep power supply noise from phase-modulating the clock.

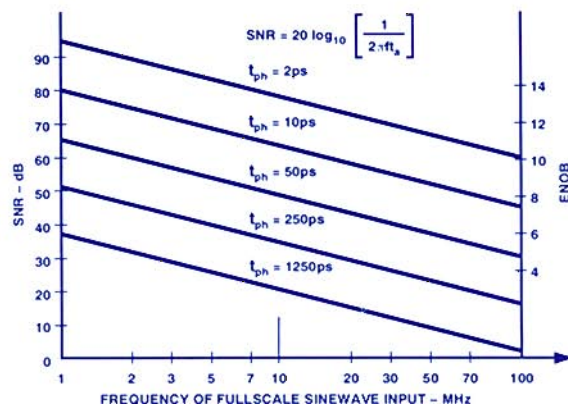
The sampling clock line should be kept away from all logic signals to prevent pickup from introducing phase noise. Equally, it should be kept away from low-level analog signals lest it corrupt them.

Q. *You have told me not to use the clock oscillator of my processor as the sampling clock source. Why not? Isn't it sensible to use the same oscillator for both, since there will then be a constant phase relationship between the signals?*

A. True. But in such cases, it is often better to use a single discrete low-noise oscillator to drive the processor clock input and the sampling clock divider *through separate buffers* (though they may share a package) than to use the oscillator in the processor. In medium-accuracy systems with low sampling rates it may be possible to use the processor's internal oscillator—but check with the diagram below).

Q. *Just how serious is this problem of noise on a sampling clock? I hardly ever see it mentioned in articles on sampled data systems.*

A. The phase noise of the sampling clock is often ignored, because the limiting factor on system performance used to be the aperture jitter of the of the sample-hold—but if we consider the system as a whole, aperture jitter is just one component of the total phase noise in the sampling clock chain. With modern sampling ADCs the aperture jitter may be less important than other components of phase noise.



The diagram shows the effect of the total phase jitter of the sampling clock on signal-to-noise ratio (SNR) or effective number of bits (ENOB). This jitter has the rms value of t_{ph} , which is made up of the root-sum-of-squares of the phase jitter on the sampling clock oscillator, the phase jitter introduced by pickup during transmission of the sampling clock through the system, and the aperture jitter of the SHA in the sampling ADC. This diagram may be somewhat unsettling, as it shows just how little phase noise is required to corrupt a high-resolution sampled-data system.

MORE ON TRIMMING

Q. *I don't have enough range to adjust the offset of my circuit—and it seems to have rather more drift than I'd expected.*

A. I'll bet the amplifier is a bipolar type and you are using its offset-trim terminals to trim other circuit voltages.

Q. *How did you guess?*

A. The range of offset adjustment of an op amp is normally 2 to 5 times the maximum expected offset of the lowest grade of the device (in some early op amps, it was much larger, but such a wide range is not ideal). If the lowest grade has a V_{os} (max) of ± 1 mV, then the likely adjustment range with the recommended circuit is ± 2 to ± 5 mV.

If the external voltage you are attempting to compensate for is larger than this (referred to the op amp's input), you will not be able to do so with the amplifier's offset-trim terminals.

Furthermore, if you are using a *bipolar-input* op amp, it is inadvisable to use these terminals for external offset correction because drift will be increased. Here's why: the input stage thermal drift is proportional to the internal offset; if this has been trimmed to a minimum, the drift will also be a minimum. If you then trim the amplifier to compensate for an external offset, drift will no longer be minimized. However, *FET-input* op amps have separately trimmed offset and drift, their offset adjustment terminals may thus be used for small system adjustments. ▣

MORE AUTHORS (Continued from page 2)

Bill Schweber (pp. 8 & 21) is a Senior Technical Marketing Engineer and Contributing Editor to *Analog Dialogue*. Besides having his BSEE and MSEE degrees, he has designed μ P-based machine controls, been a product marketing engineer, and written three textbooks. He contributes numerous articles to *Analog Dialogue* and the electronics press—many of which introduce new products to the market.



Ian Bruce (page 11), is a Senior Technical Marketing Engineer in the Marketing Communications Group in Norwood, MA. In over 5 years with Analog Devices, he has worked in design, marketing, and sales in the USA and England, his native country. Ian holds a B.Sc. degree in Electrical Engineering from Coventry College. His interests include reading, travel, and an increasingly reluctant MG sports car. [Ed.—It may be for sale.]



Walt Jung (page 13) is a Corporate Staff Applications Engineer at ADI. Earlier he consulted on applications projects, and wrote a variety of application notes and articles for *Analog Dialogue* and the trade press. He has authored ten books (e.g., *IC Op Amp Cookbook*) and hundreds of articles on linear-IC applications. Walt attended Drexel Institute of Technology, is a member of IEEE and a Fellow of the AES. He enjoys live and recorded music.



Walt Kester (page 26) is a Corporate Staff Applications Engineer at ADI. During more than 20 years at ADI, he has designed, developed, and given applications support for high-speed A/Ds, D/As, SHAs, op amps, and muxes. Besides writing many papers and articles, he prepared and edited the Notes for High-Speed, Mixed-Signal, and Advanced-Linear Design seminars. Walt has a BSEE from NC State and MSEE from Duke. He enjoys carpentry and travel.



James Bryant (page 27) is European Applications Manager for ADI, based in Walton-on-Thames, England. A graduate of the University of Leeds, he earned a B.Sc. in Physics and Philosophy. He has 22 years of applications experience at Plessey and ADI. James has published widely and diversely and served as a technical adviser to Parliament on CB radio. His various interests include amateur radio (G4CLF), collecting science fiction (>3 k volumes), hypnotism, and parapsychology. ▣



ADI FELLOW NAMED:

Carl Roberts

Carl Roberts has been named a Fellow in recognition of his innovations and leadership in semiconductor packaging at Analog Devices. In addition, he has recently been appointed as Director of Assembly Package and Process Development for Analog Devices worldwide.



For a manufacturer of precision semiconductors in a highly competitive market, packaging is a critical art, second only to the design and manufacture of the chips themselves. Since he joined the company in 1981, Carl has played the leading role in developing ADI's capability to reliably encapsulate precision analog ICs in low-cost plastic packages—which house a high percentage of the chips we manufacture. He was instrumental in developing the technique of post-burn-in solder dip, helping ADI to be one of the first companies in the industry to use it as the primary lead finish.

He has successfully solved tough packaging problems—and there are many in the semiconductor business—including compound monolithic integration at low cost, the eradication of moisture-induced failures, selective die overcoating to relieve die stress in plastic packages, and the whole new ball game of housing micro-machined sensor structures in IC packages. He has received two patents for his innovations, with more in the works.

Before joining Analog, Carl worked at Signetics as a packaging engineer; starting from scratch, he built a world-class packaging operation in Bangkok, Thailand. Earlier, he was an engineer at Polaroid on the SX-70 project—and had the distinction of having his image recorded in the second picture ever taken (by Dr. Land) with the first camera off the line. Earlier, he was a machine designer for Corning Glass Works. He studied Mechanical Engineering at Rensselaer Polytechnic Institute and Northeastern University.

Carl is married, with three children, and lives in Topsfield, Massachusetts. His hobbies (when he has the time) include chess, golf, and tennis.

Fellow, at Analog Devices, represents the highest level of advancement that a technical contributor can achieve, on a par with Vice President. Fellows will have earned universal respect and recognition from the technical community for unusual talent and identifiable innovation at the state of the art; their significant technical contributions will have had a major impact on the company; they must have demonstrated superior creative ability in product or process technology leading to commercial success.

Other attributes include roles as mentor, consultant, organizational bridge, gatekeeper, entrepreneur, teacher, and ambassador. They must also be effective as leaders of teams and contributors to team effort and in understanding the voice and needs of the customer. Carl's accomplishments and technical abilities, as well as his personal qualities, make him well-qualified for this appointment. He joins Fellows Derek Bowers (1991), Paul Brokaw (1980), Lew Counts (1984), Barrie Gilbert (1980), Jody Lapham (1988), Fred Mapplebeck (1989), Jack Memishian (1980), Wyn Palmer (1991), Mike Timko (1982), Bob Tsang (1988), and Mike Tuthill (1988). ▣

Worth Reading

WHAT'S HOT IN SPICE?

New **SPICE** Diskette. ADSpice "F", April, 1992 adds 36 models of 9 generic devices, for a total of 300 models. **FREE.** Circle 25

LINEAR DATABOOKS

Amplifier Reference Manual (1,536 pages) and **Special Linear Reference Manual** (640 pages), now available as a boxed pair, contain complete data sheets, orientation material, and selection trees and guides on all current linear-IC products. The former covers op amps, in-amps, iso amps, and comparators; the latter covers multiplier/dividers and components for signal-compression, rms-to-dc, mass storage, ATE, temperature sensing, signal conditioning, etc. **Free.** Circle 2

GUIDES

Sampling Analog-to-Digital Converter Integrated Circuits 1992: 28-page Selection Guide. Includes tutorial, application considerations, specifications and terms, and listings for 35 different models, with resolutions from 8 to 16 bits and speeds up to 20 MSPS. **Free.** Circle 26

Amplifier Products Cross-Reference Guide. 1992: 56-page guide to selecting ADI amplifiers and replacements for products of other manufacturers. Includes Ordering information; Model numbering system; Package information; Amplifier-product selection trees for instrumentation amplifiers and high-speed-, precision-, low-power-, and low-noise op amps; 33 pages of cross-reference tables for more than 3500 amplifier products; Military-aerospace amplifier information; and Sales offices and distributors. **Free.** Circle 27

BROCHURES

7B Series signal conditioners: Single-point sensor I/O optimized for process control. Illustrated 8-page brochure describes the new 7B family of low-cost modular mix-and-match input- and output signal conditioners for process control. **Free.** Circle 28

Signal-Conditioning sigma-delta a/d converters. 6-page brochure describing the AD7710-13 series (see the last issue): Principles, Devices, Applications, Worldwide sales directory. **Free.** Circle 29

Digital signal processing. A 24-page overview of Analog Devices fixed- and floating-point digital signal processors, mixed-signal processors, tools, software, support, and introduction to signal computing. **Free.** Circle 30

Signal Computing. 20-page introduction to Signal Computing (see pp. 8-10, this issue). Background, technology, algorithms, PC applications, FAX/data modems, wireless communications, digital sound, speech recognition. **Free.** Circle 31

SERIAL PUBLICATIONS

DSPatch—The DSP Applications Newsletter:

Number 23, Spring, 1992, 20 pp. Special ICASSP '92 issue: Partners in Signal Processing, describing customer applications, such as digital mobile telephones, speech recognition, multimedia, professional digital audio. Also featuring ADSP-21010 low-cost floating-point processor, EZ-KIT development tools, C language development tools, joint development agreement with H-P for submicron IC technologies. Plus: more customer applications, Q & A, BBS, distribution, workshops, current software releases, literature. **Free—while they last.** Circle 32

Analog Briefings—The Newsletter for the Defense/Aerospace Industry

Vol. 8, No. 1, 8 pp. Feature articles include Part 2 of ADI's RADTESTSM data service; Weight and pressure measurements with instrumentation amplifiers; High-speed single, dual, and quad sample-and-hold amplifiers. **Free—while they last.** Circle 33

Vol. 8, No. 2, 12 pp. Featuring: Monolithic RF track/hold amplifiers for direct IF-to-digital sampling; Updates to MIL-STD-883 (D) and MIL-M-38510 (J); Current-feedback amplifiers for high-speed applications; Definitions of analog multiplier specifications; Analog multiplier selection. **Free.** Circle 34

APPLICATION NOTES

Evaluation board for the AD7884 16-bit A/D converter, by Mike Curtin. (AN-228), 6 pp. Introduction, Link options, Power supplies, grounding, & decoupling, Analog input section, AGND buffer, Multiplexer applications, Reference section, Evaluation-board interfacing, Board layout and component overlay. **Free.** Circle 35

Evaluation board for the AD7885 16-bit A/D converter, by Mike Curtin. (AN-229), 6 pp. Similar topics to AN-228 above. **Free.** Circle 36

Considerations for selecting a DSP Processor (ADSP-2111 vs. DSP56000), by Noam Levine (AN-231), 12 pp. Introduction, Arithmetic capabilities, Data addressing, Program sequencing, Data communication, Memory resources, System considerations, Development environment, Summary. **Free.** Circle 37

Considerations for selecting a DSP Processor (ADSP-21020/ADSP-21010 vs. TMS320C30), by Dan Ash (AN-235), 12 pp. Introduction, Arithmetic capabilities, Data addressing, Program sequencing, External memory, Assembly language, Benchmarks, Summary, References. **Free.** Circle 38

Bootstrapped IC substrate lowers distortion in JFET op amps, by Walt Jung (AN-232), 4 pp. Introduction, The problem of nonlinear input capacitance, Minimizing nonlinear input-capacitance effects, Design factors, Performance, Unbuffered bootstrap, Application tips, References. **Free.** Circle 39

ADI ENGINEERS IN THE TRADE PRESS

(Reprints not available from the Analog Devices Literature Center)
"Voltage-reference circuit boasts low noise," by Adolfo Garcia. *EDN*, March 30, 1992 (p. 136+). [OP-177]


"Optimize the stability of fast op amps," by Joe Buxton. *Microwaves & RF*, April, 1992 (p. 74+).

"Improve noise analysis with op-amp macromodule," by Joe Buxton. *Electronic Design*, April 2, 1992 (p. 73+). [OP-27]

"Paralleled amplifiers drive loads quietly," by Moshe Gerstenhaber and Mark Murphy. *EDN*, April 23, 1992 (p. 171+). [AD829]

"Design and Layout of a video graphics system for reduced EMI," by Bill Slattery and John Wynne. *Interference Technology Engineers' Master*, 1992 (p. 40+).

"Surround and other sounds," by Dan Parks. *Video shopper*, May, 1992 (p. 74+).

"Ground acts as thermocouple reference," by Adolfo Garcia. *EDN*, May 21, 1992 (p. 174). [AD592, OP-177, REF-01] 

An Eclectic Collection of Miscellaneous Items of Timely and Topical Interest. Further Information on Products Mentioned Here May Be Obtained Via the Reply Card.

STOP PRESS—NEW PRODUCTS:

Monolithic ICs:	Circle
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• Op Amp: Dual 9-MHz, 250- μ V offset, 22 V/ μ s SR, OP-285 . . .	45
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• 883B versions of AD811 op amp, AD620 in amp, and three n-uple sample holds: AD781 (n=1), AD682 (n=2), AD684 (n=4) . . .	59

ERRATA & CHANGES ••• ADSP-2101 data sheet (C1404c) has two errors in PQFP package dimension table, p. 27. TYP values for B and e (inches) should be .012 and .026, respectively; mm values are OK ••• The ADSP-2111 data sheet (C1605) has an error in PGA pin configurations, p. 28. PGA number B6 should be designated HD4; also, the Ordering Guide, p. 32, omits the part number of extended temperature range, non-883B devices: ADSP-2111TG-52, with 13-MHz instruction rate, and 100-pin grid-array package; finally, in the plot of internal power vs. frequency in Fig. 18, p. 12, the RH endpoint, 445 mW, is correctly labeled, but the curve is incorrectly plotted with too steep a slope ••• AD9950 300-MSPS Phase Accumulator—(C1475, page 2) correct +V_S Supply Current specs are: at +25°C, 16 mA typical, 22 mA max; and for full temperature range, 25 mA max ••• AD9712B/AD9713B data sheet (C1635), spec tables: In the Reference Control Amp section, min/max values are -1.11 and -1.25 V at +25°C, -1.09 and -1.27 over full temperature; also, in the Power Supply section, power supply rejection ratio is 125 μ A/V max ••• AD2890 data sheet (C1653), page 3—t_g should be 600 ns min; page 6—maximum read time computation at the top of column 2 should read: (600+(12 \times 500)+600+100)=7.30 μ s ••• HTS-0010 data sheet (C779), page 1 and page 6—delete references to HTS-0010SD/883 ••• 1992 Data Converter Reference Manual (Vol. II), pages 2-776 and 11-46, diagram for J-28 leaded ceramic chip carrier—short corner should be at upper left, not upper right ••• If you attended the 1992 Advanced Linear Design seminar in spring, 1992 and were rewarded with a copy of the first printing of the 1992 Amplifier Applications Guide, you should have received an Errata sheet in the mail recently. If one hasn't arrived, get in touch with our Literature Center. Even if you didn't attend the seminar, you can still purchase a copy of this 648-page book—in a new edition with those errors corrected; use the book ordering card.

PRODUCT NOTES ••• Products newly available in SOIC: AD811, SSM-2017 (now also in plastic DIP), SSM-2018, SSM-2141, SSM-2142, SSM-2143, SSM-2404 ••• The AD7568 octuple 12-bit DAC is now available in PLCC ••• The DAC-8412 and -8413 prime grade (1/2 LSB) are now available in 28-pin plastic DIPs. /883 versions are also available in ceramic DIPs and LCCs ••• AD7578 and AD7582 commercial and industrial grades are now offered for -40 to +85°C; they are also now available in cerdip ••• Evaluation boards are available for many of our high-performance ICs. If you're interested, ask! ••• The ADSP-2101 12.5-MHz Emulator can be upgraded to run at 16.67 MHz. Get in touch with Analog Devices DSP Marketing [(617) 461-3881] for information ••• Software for RTI-800 Series data-acquisition cards for PCs is now compatible with Borland's Turbo C++ and Borland C++ (running under DOS). For information call Analog Devices. In the US: 1-800-4-ANALOG ••• The AD536 and AD636, when used in the dB mode, require +3500 ppm/°C resistors for temperature compensation. These resistors are available from PRECISION RESISTOR CO., of Largo, Florida—telephone (813) 541-5771, FAX (813) 546-9515, Telex 821788 ••• The AD633 low-cost analog multiplier can be easily used as a divider, using an external 10-V reference. Consult ADI's nearest Applications Engineer ••• A design for a low-cost, high-performance 4-channel stereo audio mixer exceeding MPC specifications for use in multimedia applications exists as an "Applications Corner" note. Consult Analog Devices Applications.

MILITARY, HI-REL, AND STANDARDS ••• Class S: For a discussion and listing of more than 175 space-qualified products from Analog Devices, call (408) 562-7197 or (408) 562-7458, or FAX (408) 727-1853 ••• Standard military drawings: Recent amplifier families released on SMDs include AD790 (5962-91505), AD827 (-92117), AD840 (-89640), AD841 (-89641), AD842 (-89642), AD843 (-90980), AD824 (-88539), AD826 (-90894), AD825 (-87719), and AD713 (-90633). Four versions of the AD2S80 monolithic R/D converter are on drawing 5962-90962. Recently added CMOS data converter families include AD7821 (5962-89518), AD7846 (-89697).

SHOWS, etc. ••• In late '92, see us at these shows: DSPWorld Expo '92, Cambridge MA, November 3, 1992; Comdex Fall '92, Las Vegas NV, November 16-20. In Spring, 1993, look forward to seeing us at AES (Europe), ICASSP, and Comdex.

PATENTS ••• 4,591,897 to Stephen Edelson for System for generating a display of graphic objects over a video camera picture ••• 4,933,572 to Douglas Smith and Derek Bowers for Dual mode voltage reference circuit and method ••• 5,055,843 to Paul Ferguson, Apparaj Ganagan, and Robert Adams for Sigma-delta modulator with distributed prefiltering and feedback ••• 5,073,633 to Derek Bowers for Instrumentation amplifier with single-supply capacity and simplified gain equation ••• 5,077,494 to Derek Bowers and Douglas Smith for Wide temperature range MESFET logic circuit ••• 5,084,753 to Thomas Goida and Carl Roberts for Packaging multiple chips on a single leadframe ••• 5,087,889 to James Butler for Area-efficient cascode driver circuit ••• 5,087,894 to Lawrence DeVito and Paul Brokaw for Monolithic interface circuit for linear variable differential transformers ••• 5,091,701 to James Butler for High-efficiency cross-coupled folded cascode circuit ••• 5,095,274 to Paul Brokaw for Temperature-compensated apparatus for monitoring current having controlled sensitivity to supply voltage ••• 5,097,223 to Mark Alexander for Current feedback audio power amplifier ••• 5,101,126 to James Butler and Douglas Smith for Wide dynamic range transconductance stage ••• 5,103,281 to Peter Holloway for MOS-cascoded bipolar current sources in non-epitaxial structure ••• 5,111,431 to Douglas Garde for Register forwarding multi-port register file ••• 5,113,362 to Stephen Haraton and Judson Leonard for Integrated interpolator and method of operation ••• 5,115,202 to James E. C. Brown for Chopper-stabilized amplifier with spread-spectrum clocking ••• 5,119,094 to Paul Brokaw for Termination circuit for an R-2R ladder that compensates for the temperature drift caused by different current densities along the ladder, using one type of bipolar transistor ••• 5,120,990 to Gregory Koker for Apparatus for generating multiple phase clock signals and phase detector therefor ••• 5,124,596 to Scott Wurcer for Single-temperature-trimmable FET input circuit having active channel segments of different areas ••• 5,124,648 to Spencer Webb and Paul Brokaw for Single winding saturable core magnetometer with field nulling ••• 5,126,586 to Barrie Gilbert for Wideband differential voltage-to-current converters ••• 5,126,653 to Apparaj Ganagan and Robert Libert for CMOS voltage reference with stacked base-to-emitter voltages ••• 5,136,184 to Kenneth Deery for Fast-acting current comparator.

IN THE LAST ISSUE

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Editor's Notes, Authors

IF stages are going digital for both analog and digital signals

Monolithic sigma-delta converters offer 21-bit resolution (AD771X)

Applying a high-performance operational amplifier (AD811)

What's hot in SPICE:

An analog-multiplier SPICE macromodel (AD734)

New-Product Briefs:

Dual and quad low-dissipation 4-MHz JFET op amps (OP-282/482)

Low-cost amplifiers for instrumentation in SO-8 (AD620, AD626)

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12-bit, 20-MSPS high-performance hybrid (AD9034)

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Monolithic R/D converter has high-performance velocity output (AD2583)

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Line driver/receiver for RS-232, RS-422 is -5-V powered (AD7306)

Differential analog line receiver for SSM-2142 transmitter (SSM-2143)

Quad audio switch has 4 independent "clickless" SPSTs (SSM-2404)

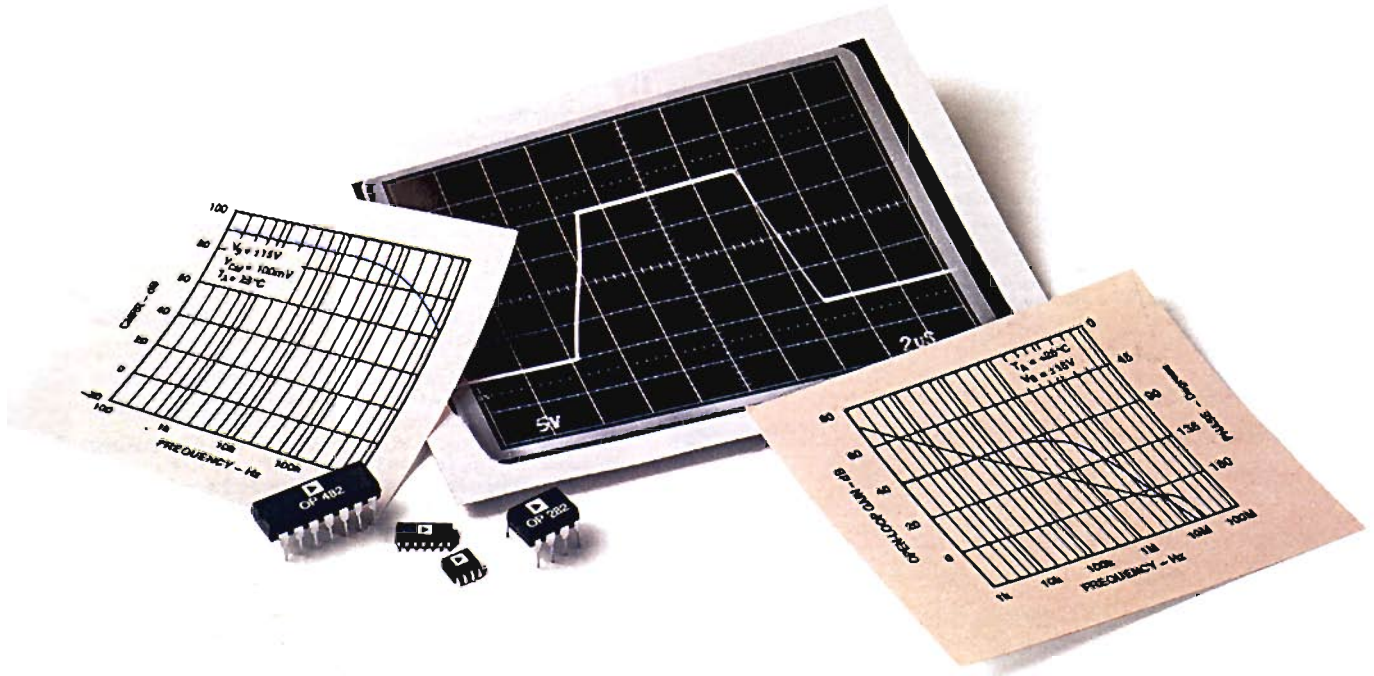
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